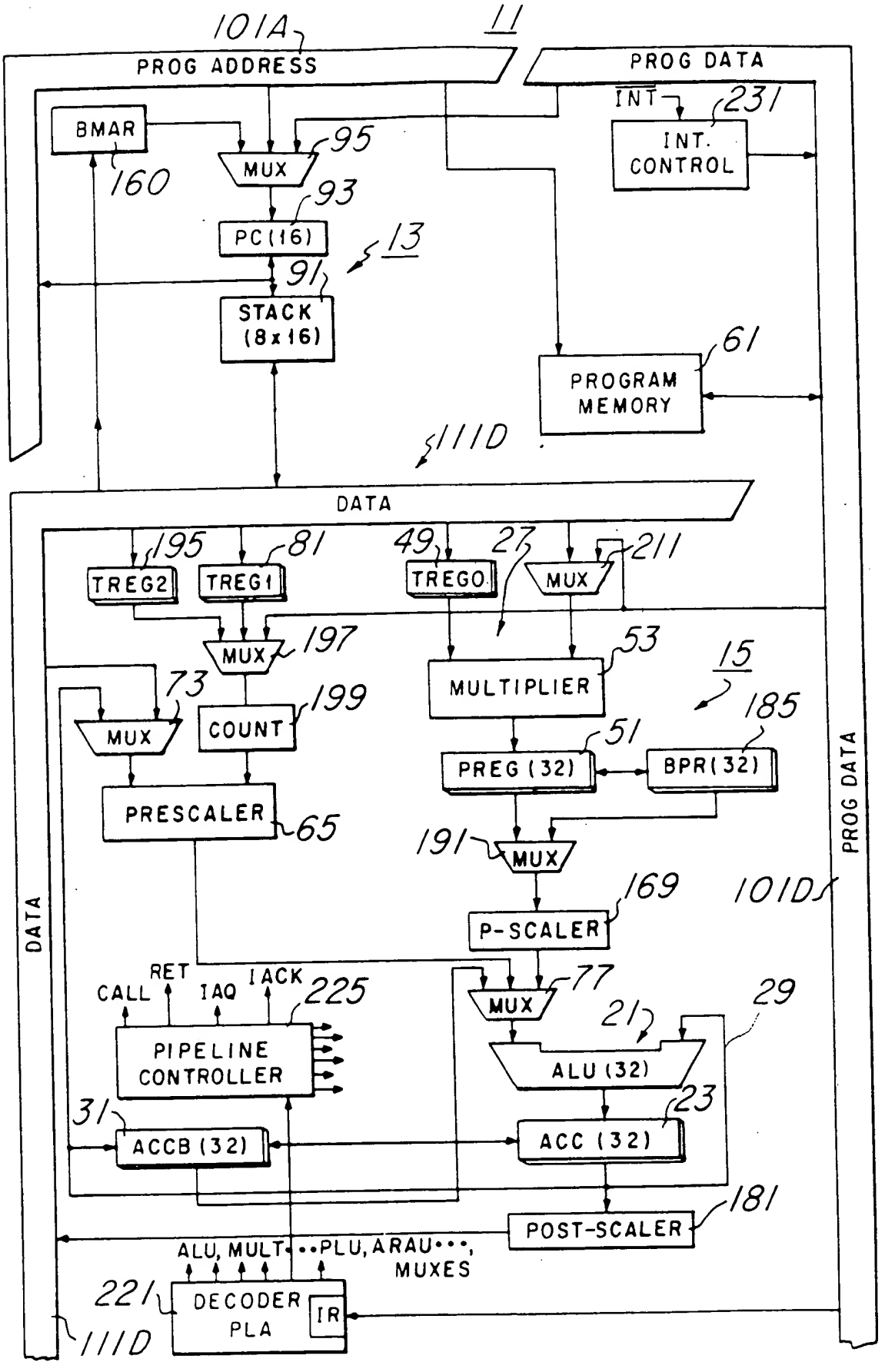

JOIN FIG.1b

Fig. 1a

0044-6502-8222950

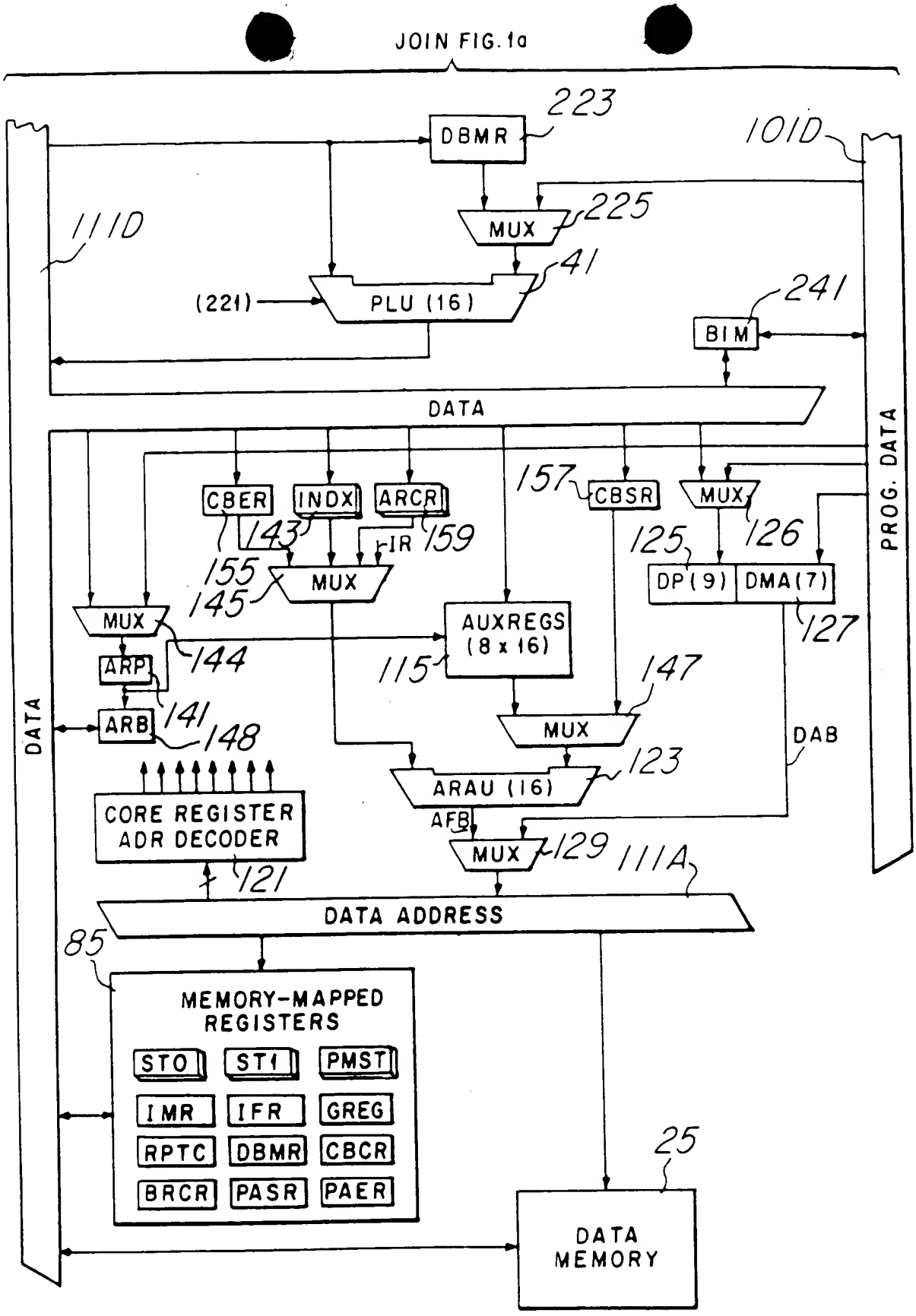

Fig. 1b

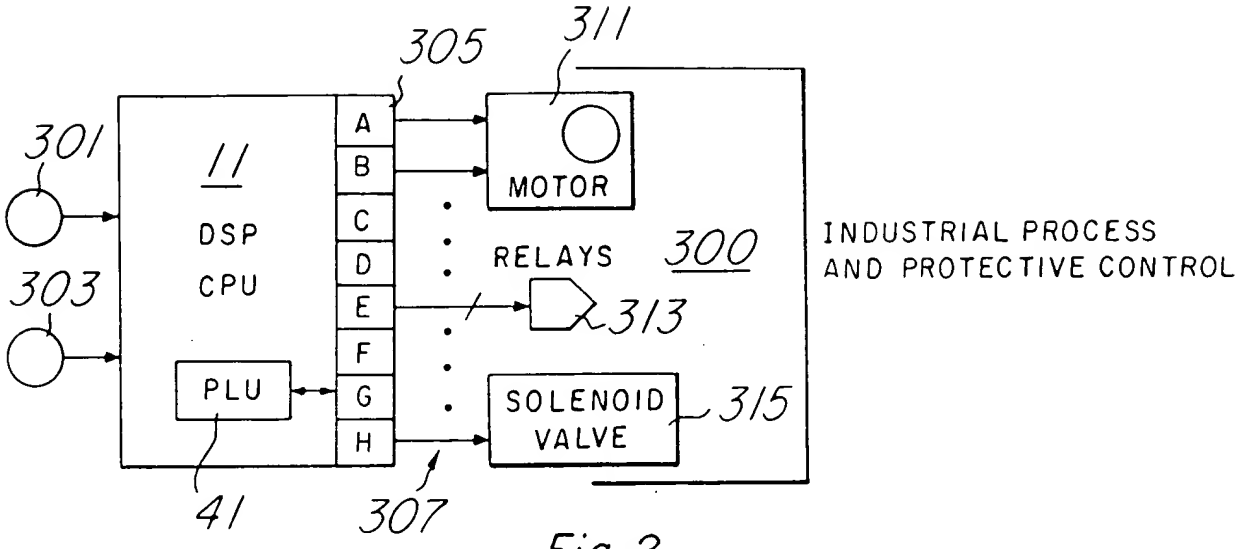
305
311
301
11
DSP
CPU
303
PLU
41
A
B
C
D
E
F
G
H
MOTOR
RELAYS
300
313
SOLENOID
VALVE
315
307
INDUSTRIAL PROCESS
AND PROTECTIVE CONTROL

Fig. 2

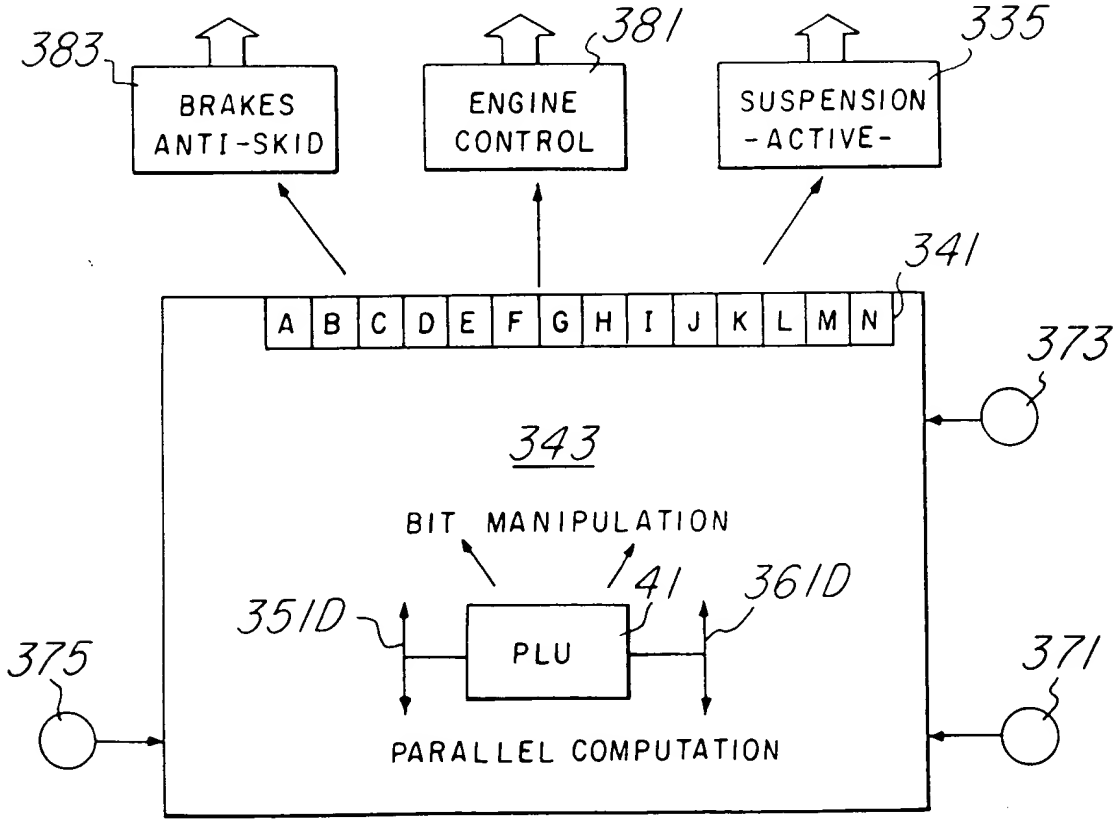
383
BRAKES
ANTI-SKID
381
ENGINE
CONTROL
335
SUSPENSION
-ACTIVE-
341
A B C D E F G H I J K L M N
373
343
BIT MANIPULATION
41
3510
3610
PLU
375
371
PARALLEL COMPUTATION

Fig. 3

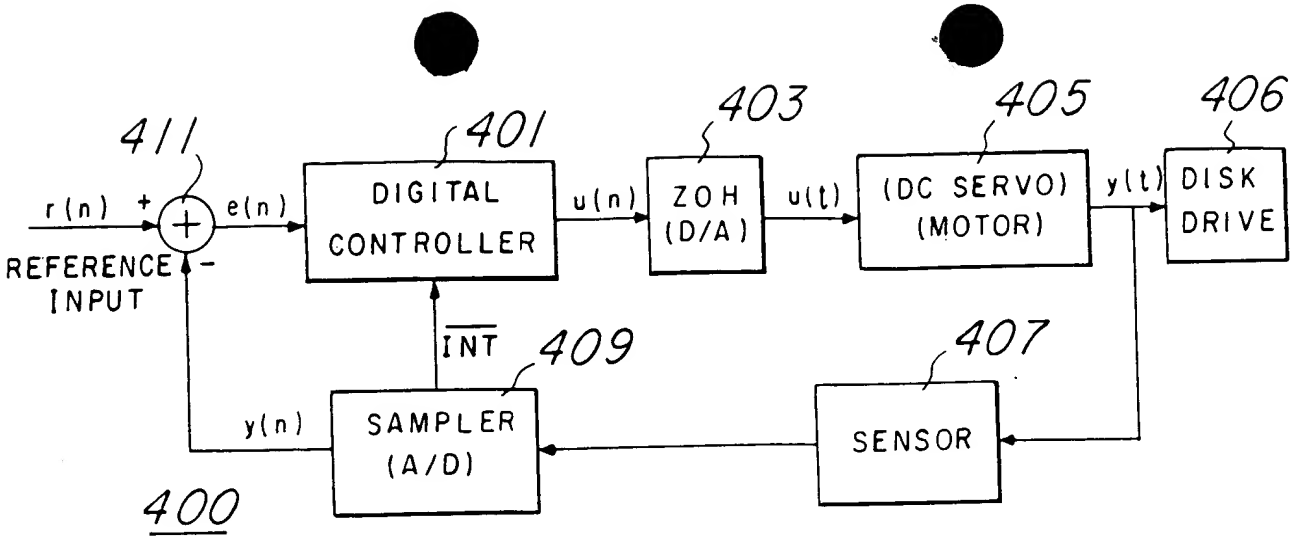

Fig. 4

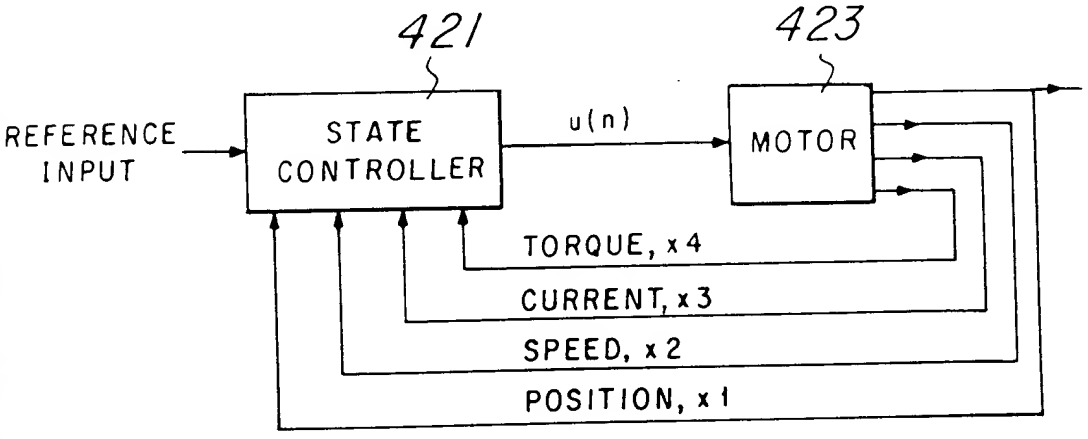

Fig. 5

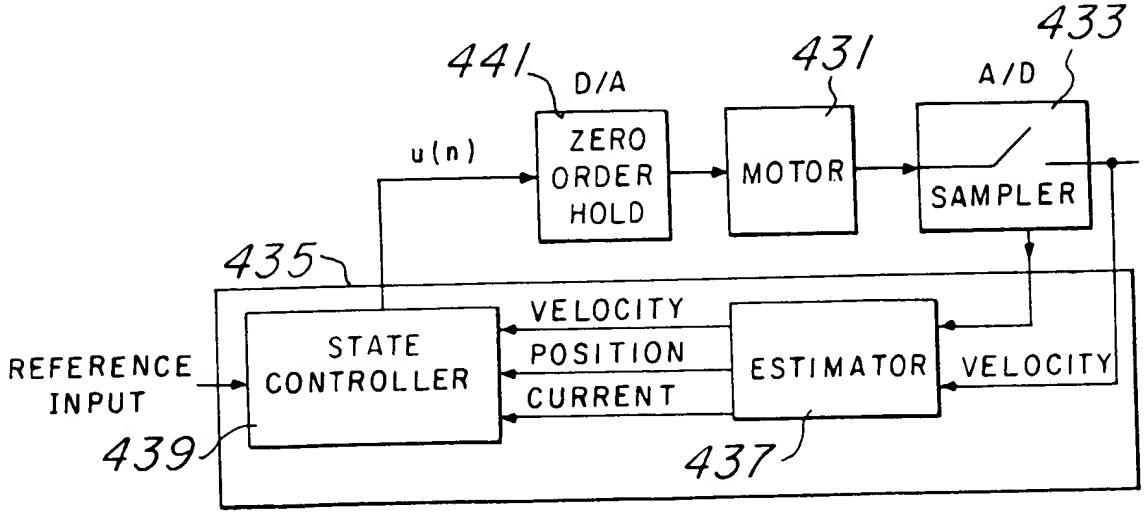

Fig. 6

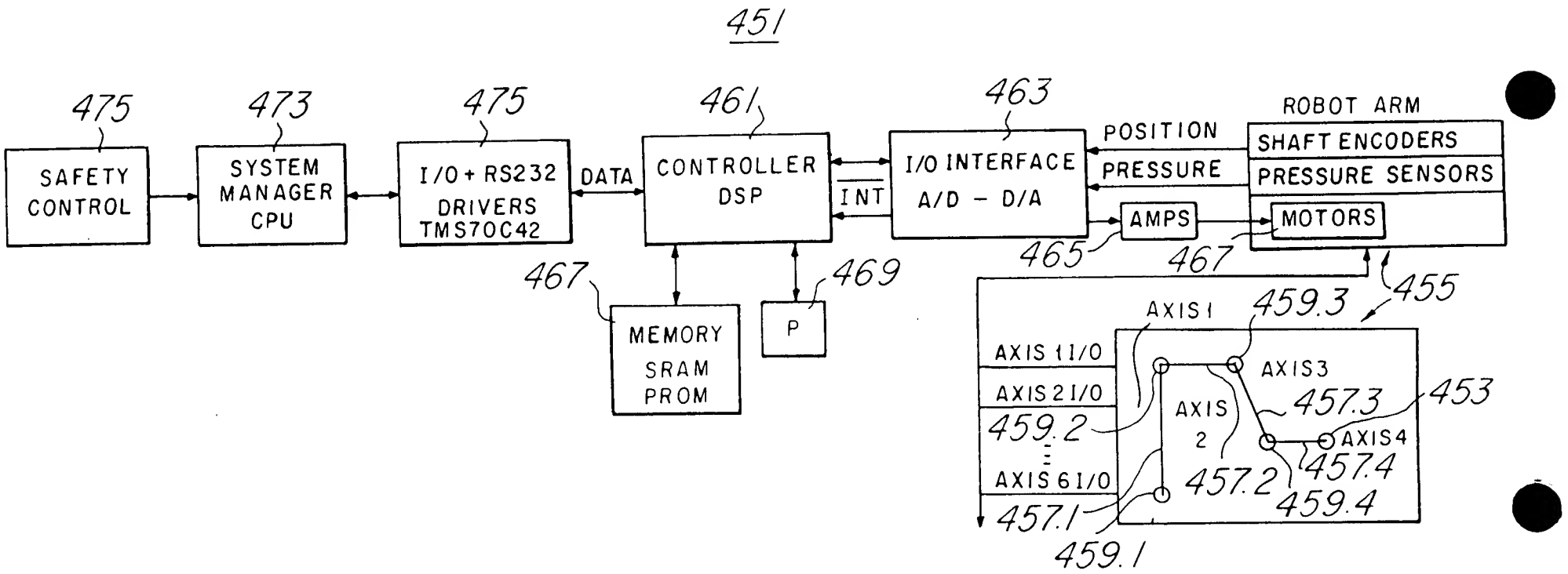
451
475
SAFETY CONTROL
473
SYSTEM MANAGER CPU
475
I/O + RS232 DRIVERS TMS70C42
DATA
461
CONTROLLER DSP
INT
463
I/O INTERFACE A/D - D/A
POSITION
PRESSURE
ROBOT ARM
SHAFT ENCODERS
PRESSURE SENSORS
AMPS
MOTORS
465
467
455
459.3
AXIS 1
AXIS 1 I/O
AXIS 2 I/O
459.2
AXIS 6 I/O
457.1
459.1
AXIS 3
AXIS 2
457.3
453
AXIS 4
457.4
457.2
459.4
467
MEMORY SRAM PROM
469
P

Fig. 7

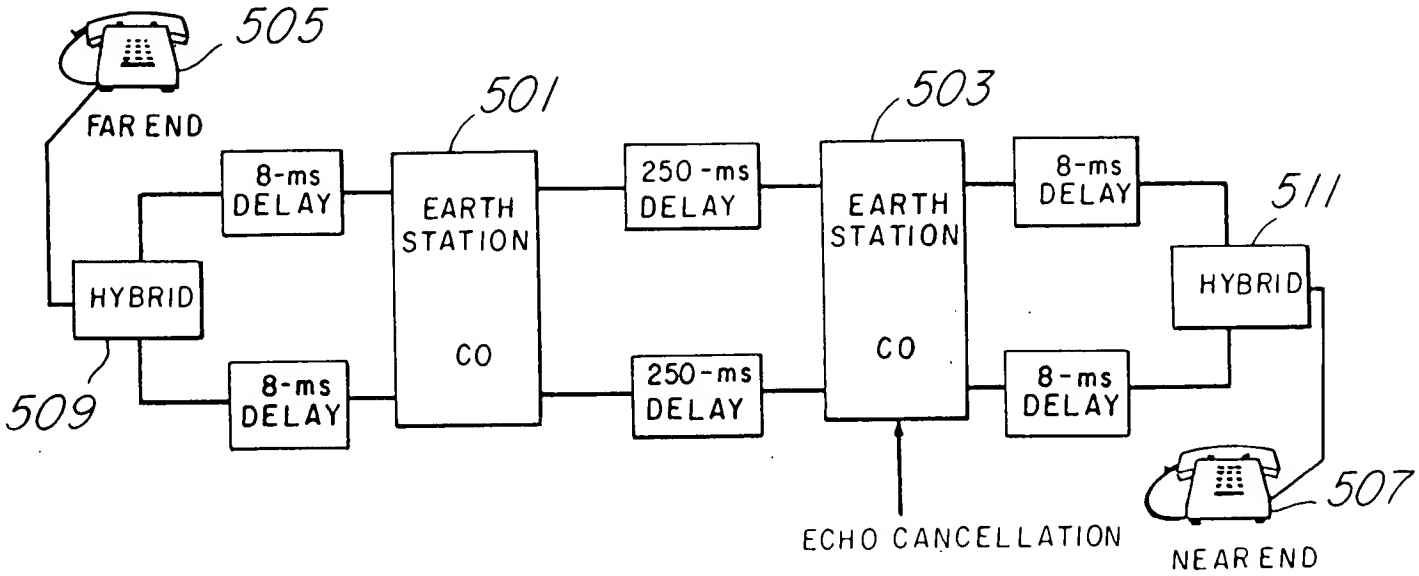
505
FAR END
501
503
8-ms DELAY
EARTH STATION
CO
250-ms DELAY
EARTH STATION
CO
8-ms DELAY
511
HYBRID
HYBRID
509
8-ms DELAY
250-ms DELAY
8-ms DELAY
507
ECHO CANCELLATION
NEAR END

Fig. 8

00T60"82229960

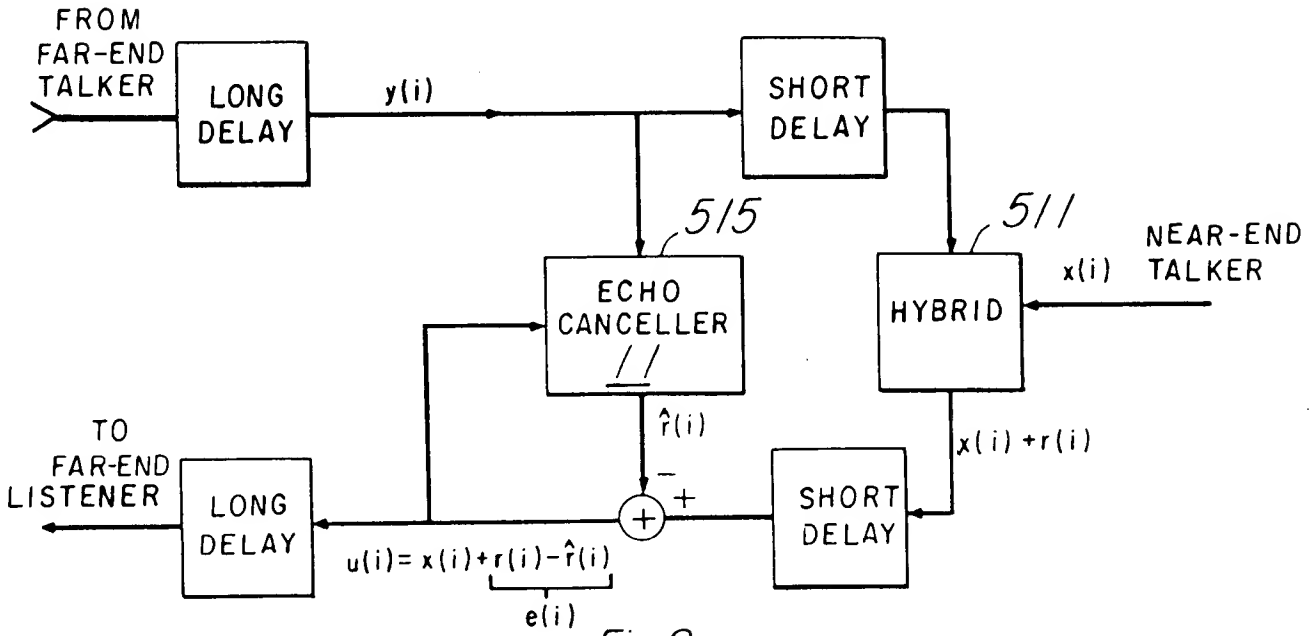

Fig.9

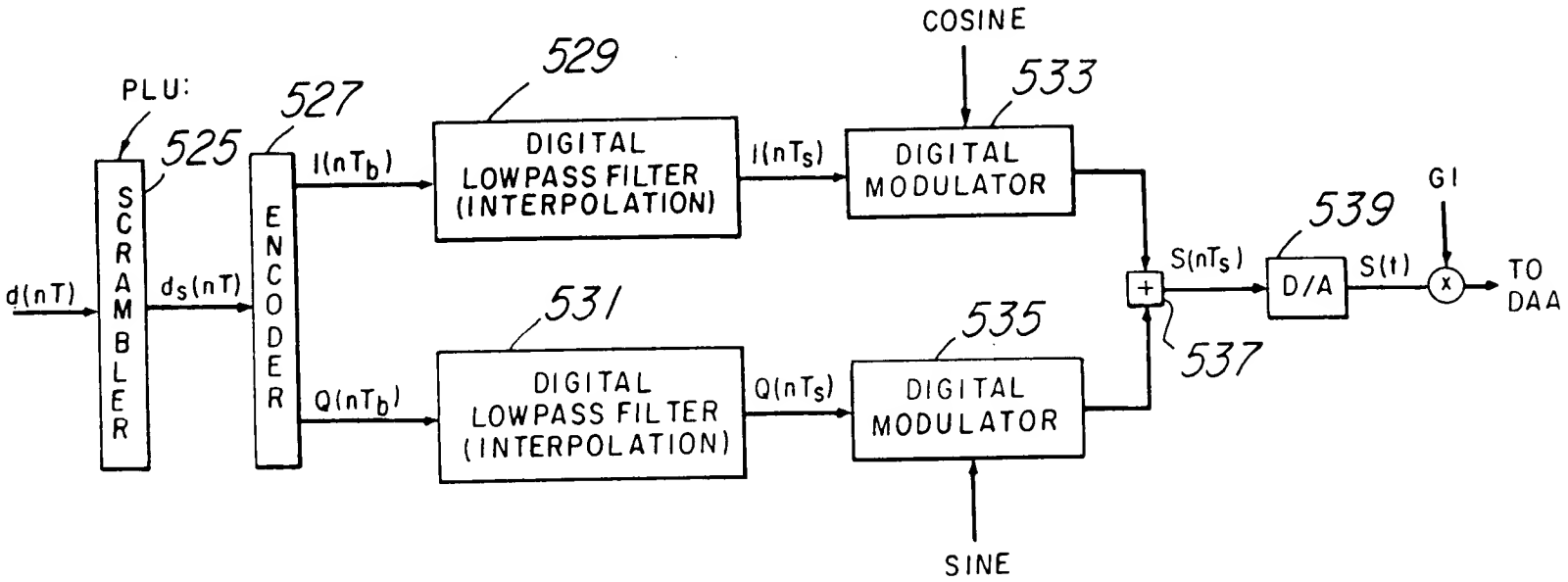
PLU:
525
527
529
531
533
535
537
539
SCRAMBLER
ENCODER
d(nT)
ds(nT)
I(nTb)
Q(nTb)
DIGITAL LOWPASS FILTER (INTERPOLATION)
DIGITAL LOWPASS FILTER (INTERPOLATION)
I(nTs)
Q(nTs)
COSINE
SINE
DIGITAL MODULATOR
DIGITAL MODULATOR
+
S(nTs)
D/A
S(t)
GI
X
TO DAA

Fig. 10

DOHT60" 8229960

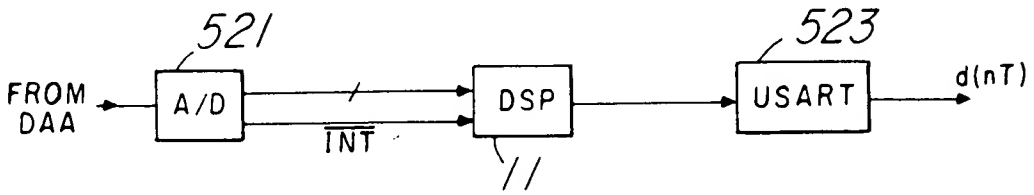

Fig. 11

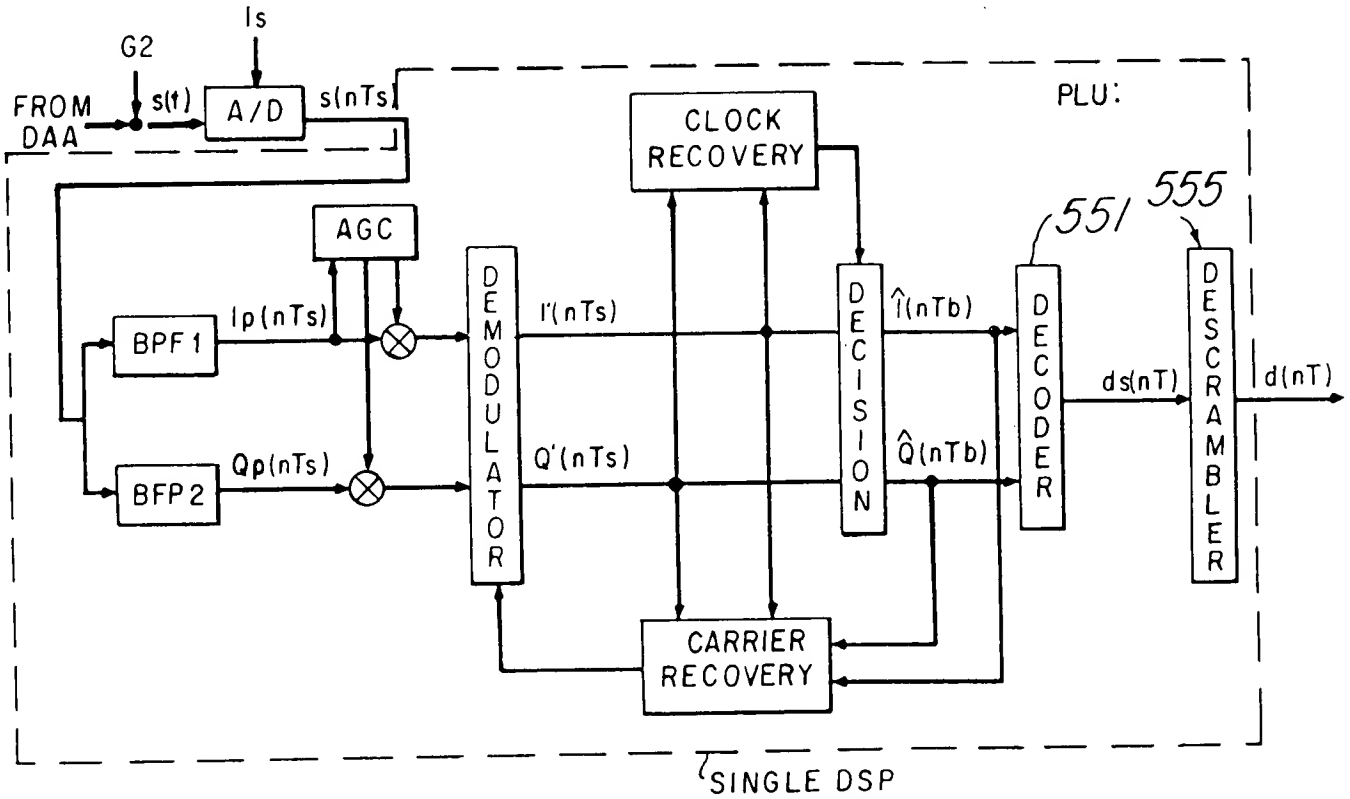

Fig. 12

00T60"8229960

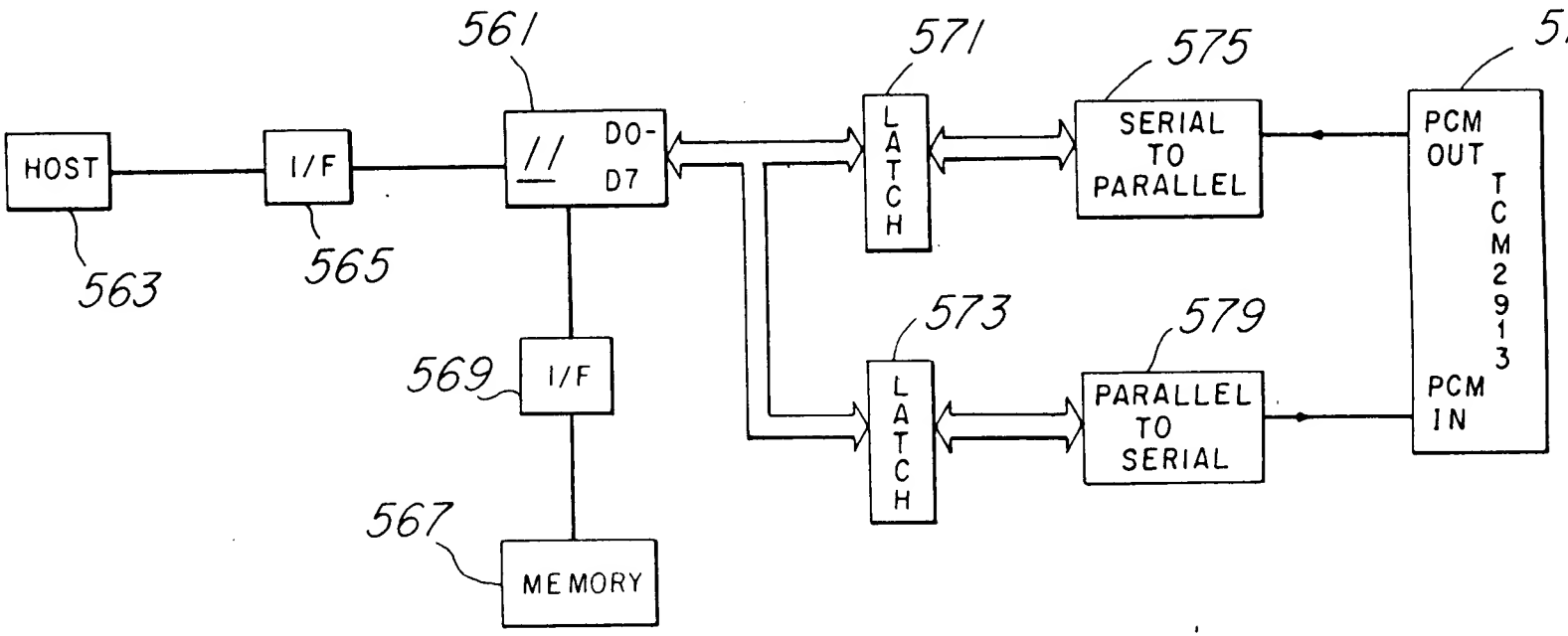

Fig. 13

00T60"8222960

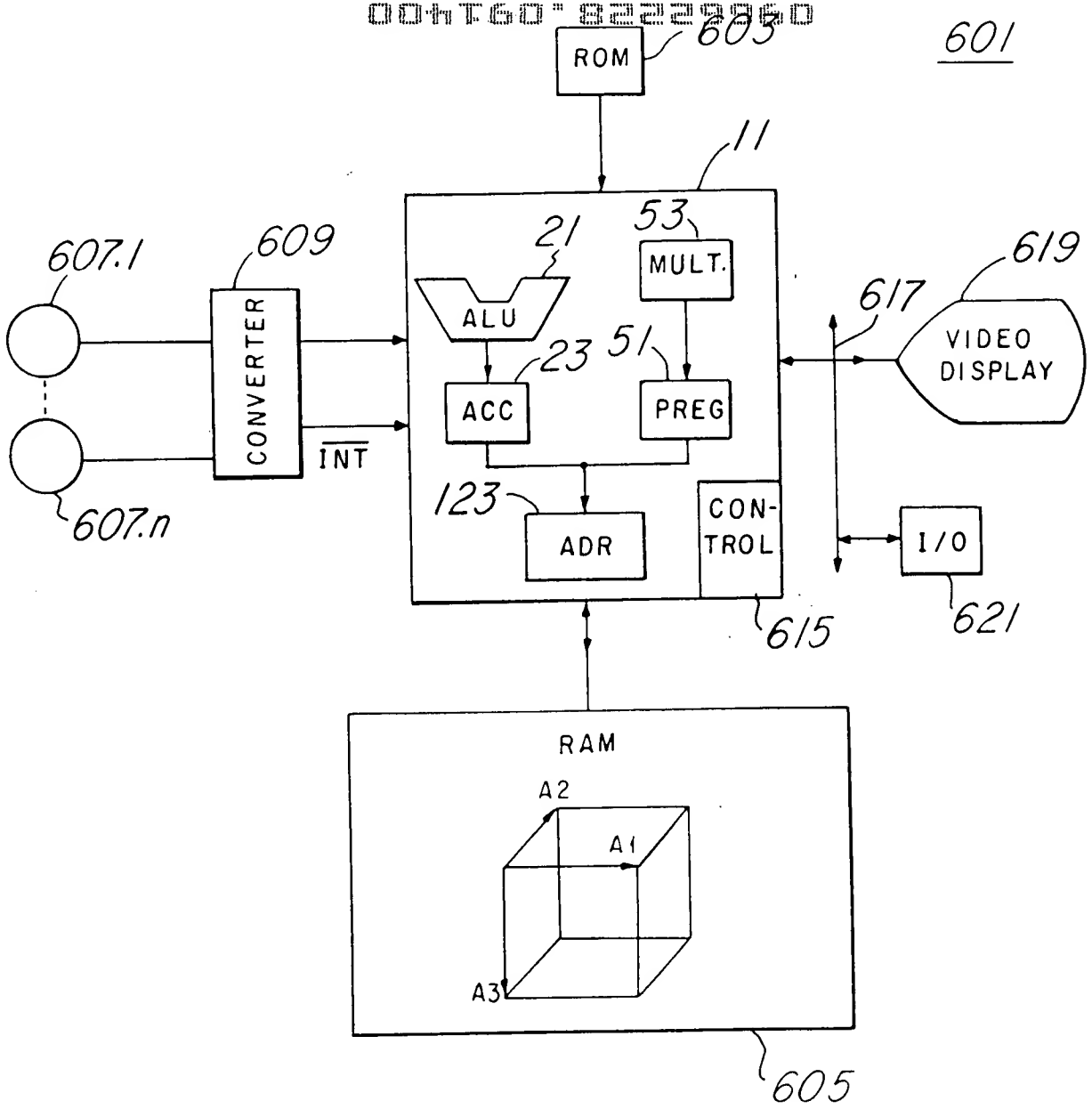

Fig. 14

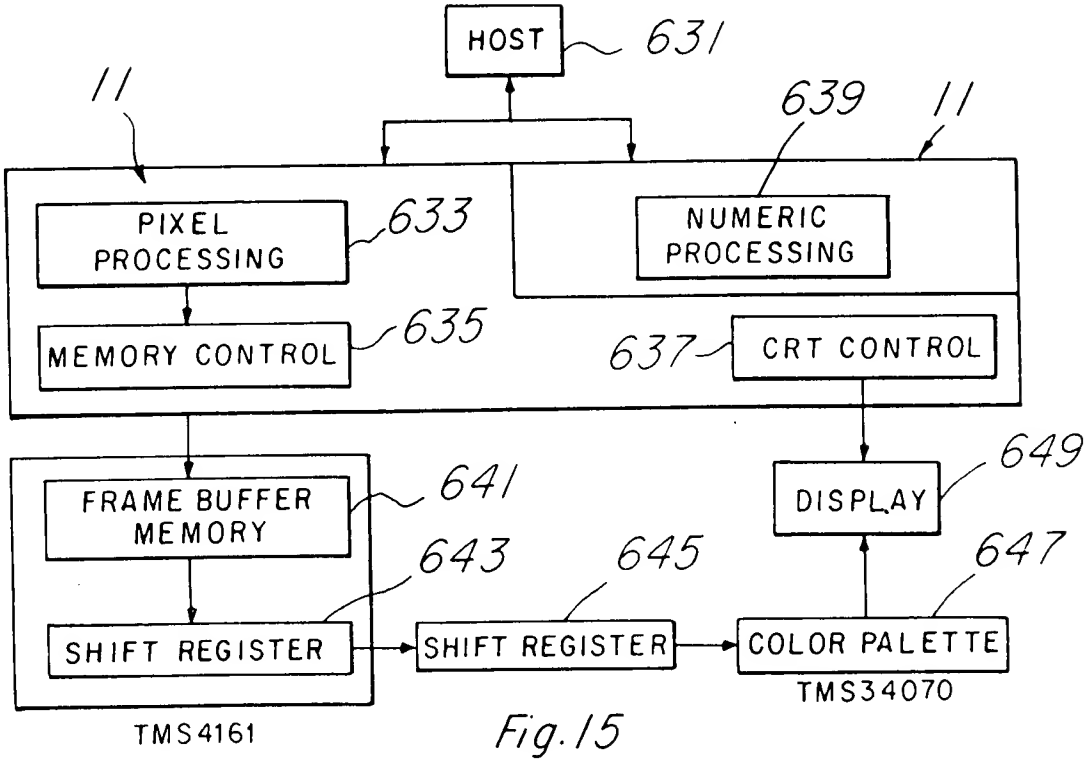
HOST
631
11
639
11
PIXEL PROCESSING
633
NUMERIC PROCESSING
MEMORY CONTROL
635
637
CRT CONTROL
649
FRAME BUFFER MEMORY
641
DISPLAY
643
645
647
SHIFT REGISTER
SHIFT REGISTER
COLOR PALETTE
TMS34070
TMS4161

Fig. 15

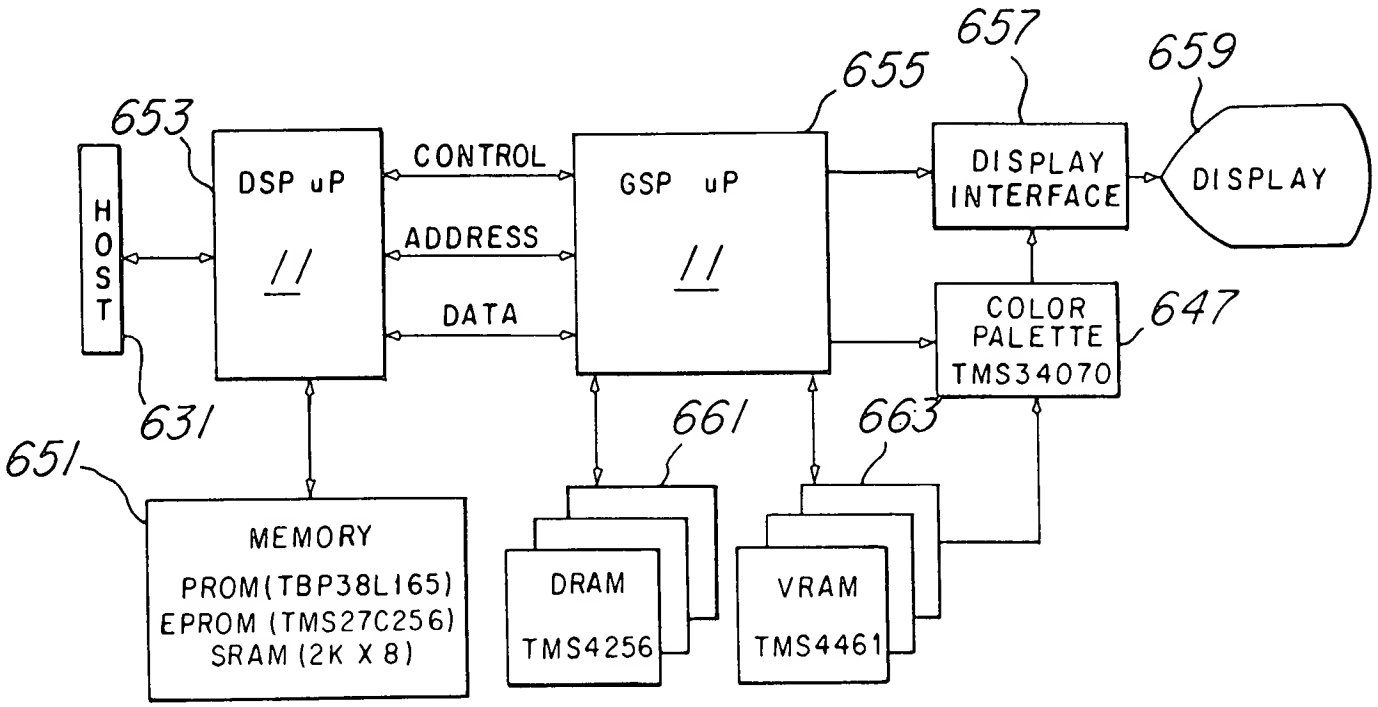
653
655
657
659
HOST
DSP uP
//
CONTROL
ADDRESS
DATA
GSP uP
//
DISPLAY INTERFACE
DISPLAY
COLOR PALETTE TMS34070
647
631
651
661
663
MEMORY
PROM(TBP38L165)
EPROM (TMS27C256)
SRAM (2K X 8)
DRAM
TMS4256
VRAM
TMS4461

Fig. 16

DOHT60"8229960

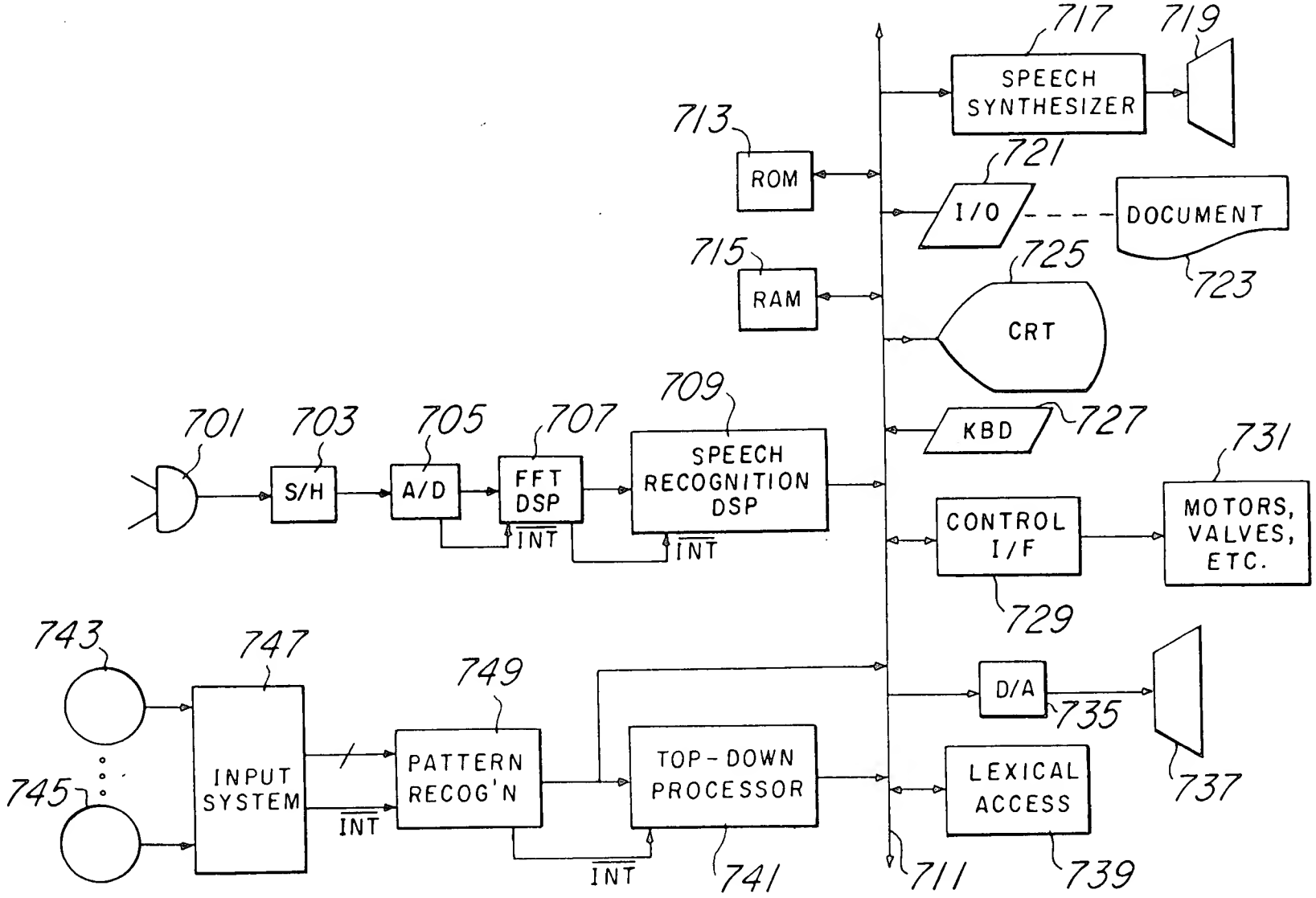

Fig.17

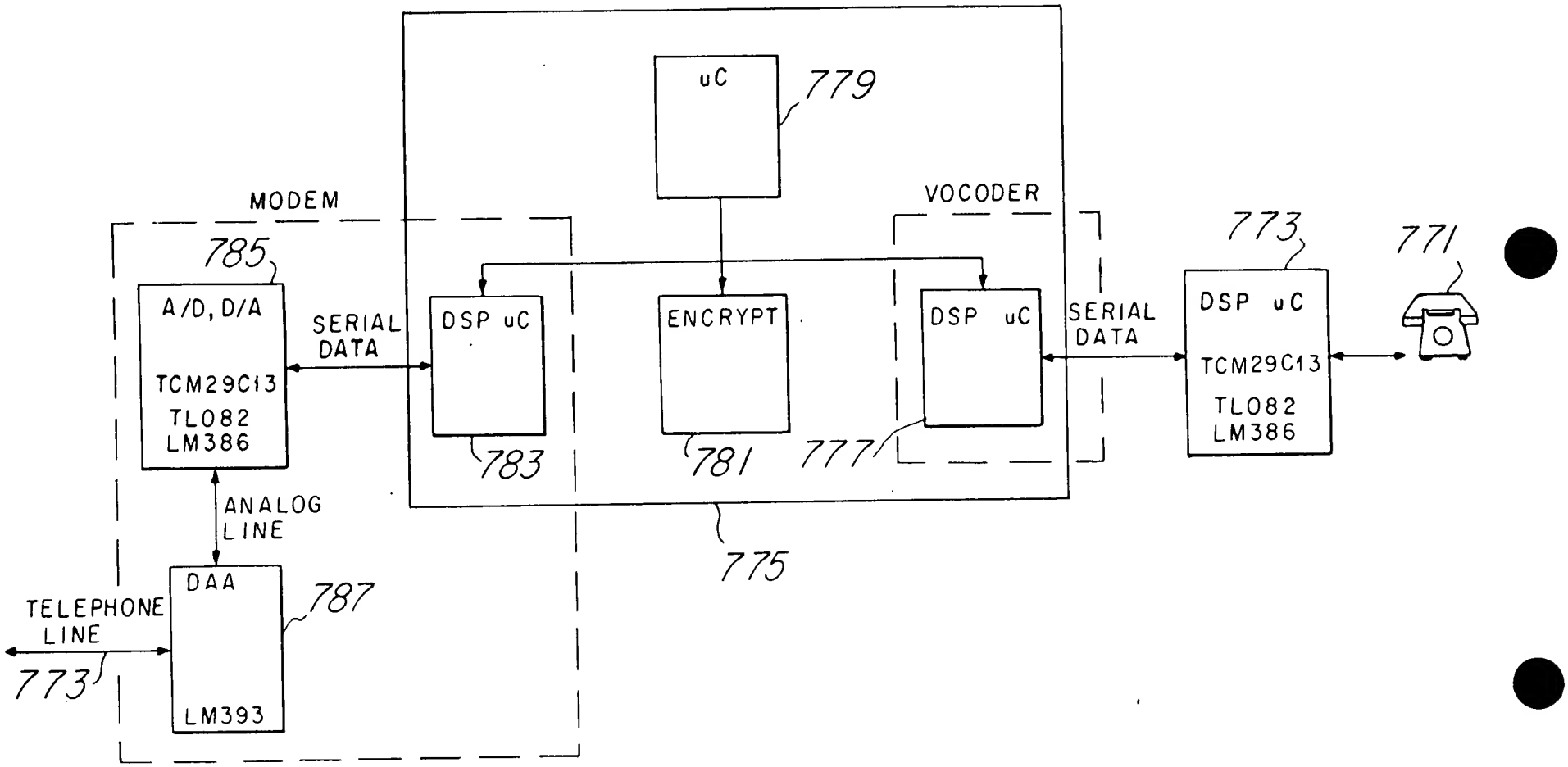
uC
779
MODEM
VOCODER
785
773
771
A/D, D/A
TCM29C13
TL082
LM386
SERIAL DATA
DSP uC
ENCRYPT
DSP uC
SERIAL DATA
DSP uC
TCM29C13
TL082
LM386
783
781
777
ANALOG LINE
775
DAA
787
TELEPHONE LINE
773
LM393

Fig. 18

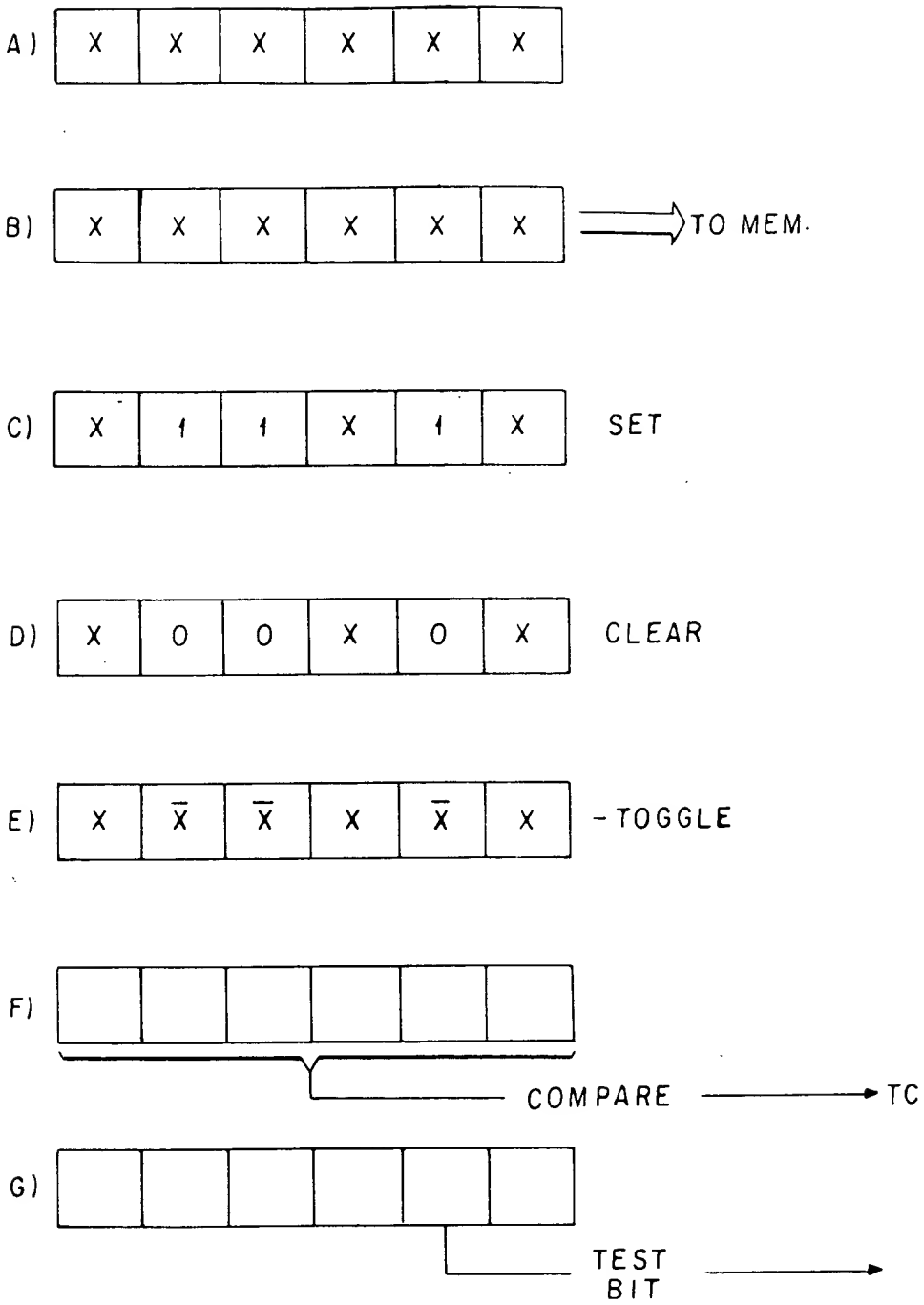
A)
X X X X X X
B)
X X X X X X
TO MEM.
C)
X 1 1 X 1 X
SET
D)
X 0 0 X 0 X
CLEAR
E)
X $\overline{X}$ $\overline{X}$ X $\overline{X}$ X
-TOGGLE
F)
COMPARE
TC
G)
TEST
BIT

Fig. 19

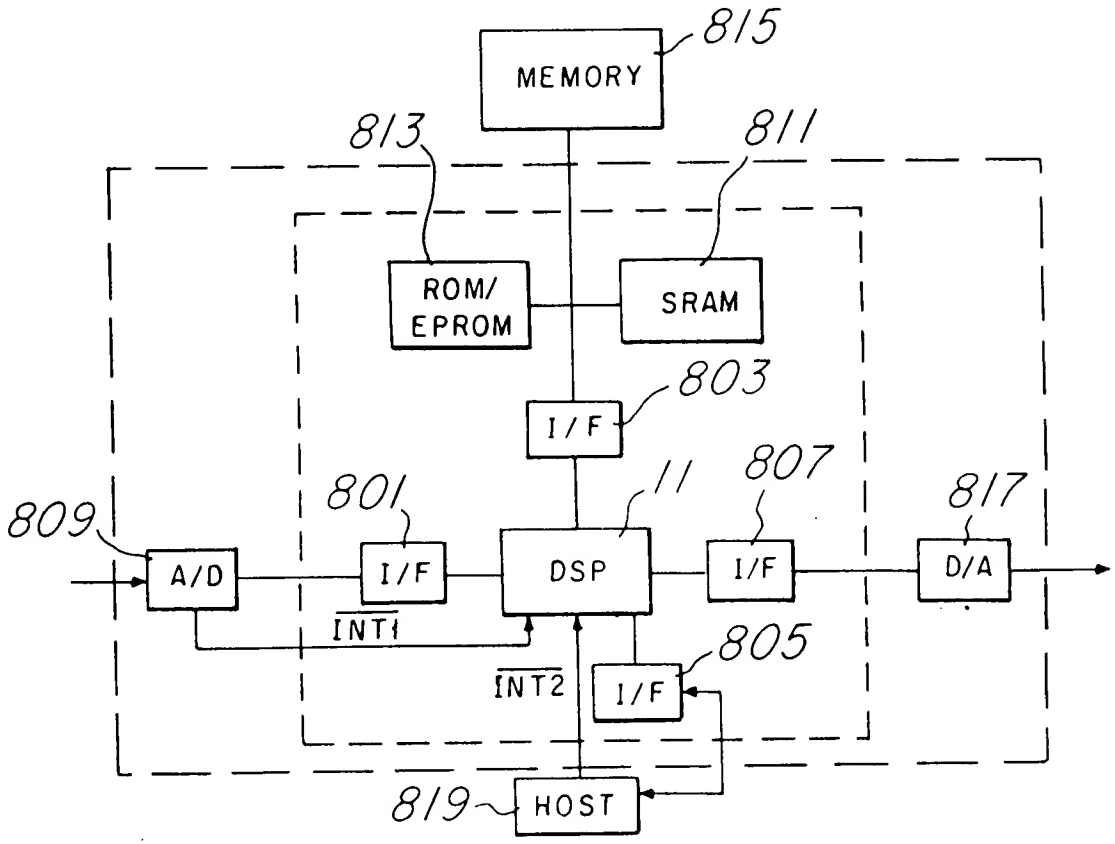
MEMORY
815
813
811
ROM/
EPROM
SRAM
803
I/F
801
11
807
817
809
A/D
I/F
DSP
I/F
D/A
INT1
805
INT2
I/F
819
HOST

Fig. 20

0960200 0960400

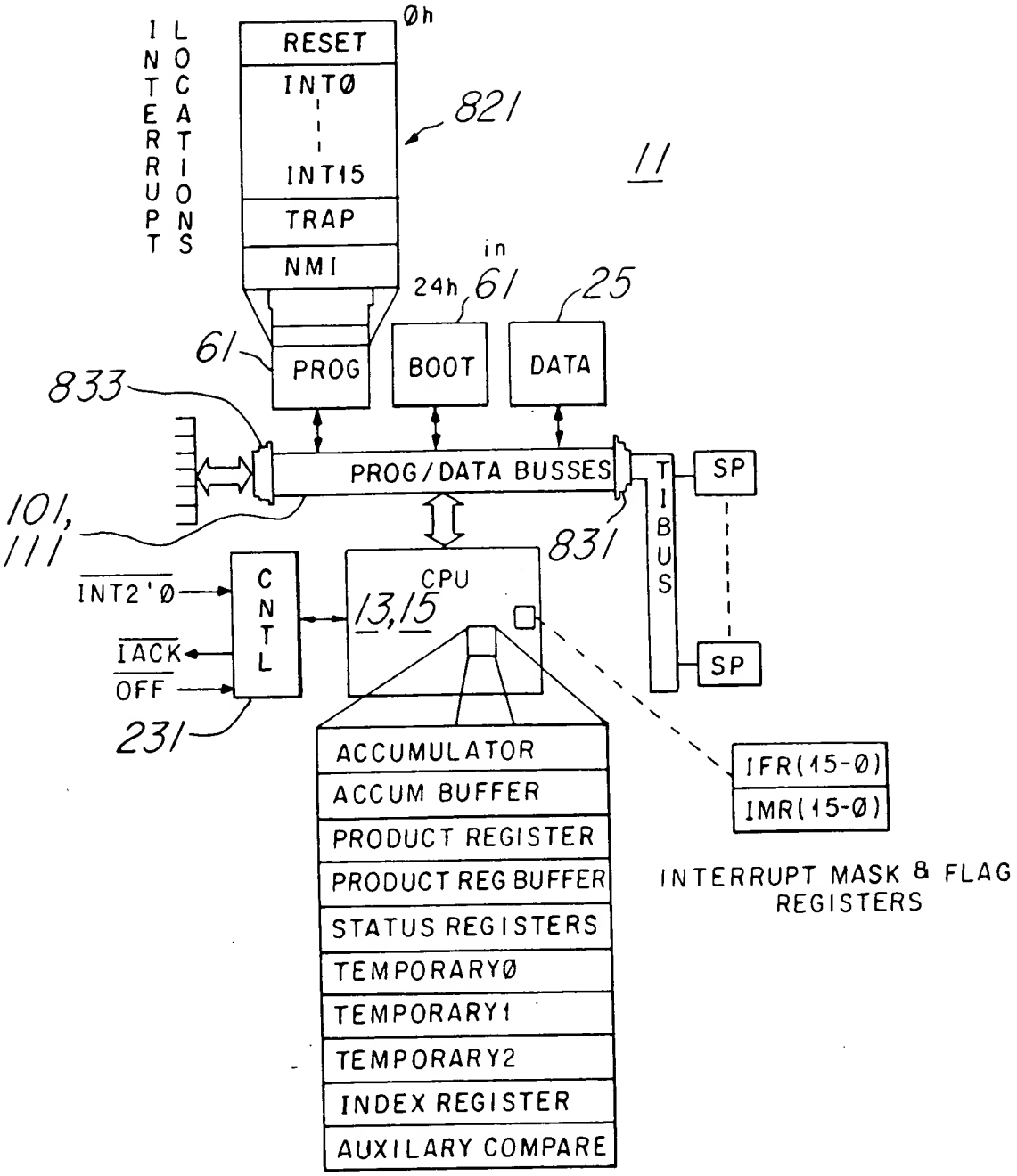

Fig. 21

0050200.0054600

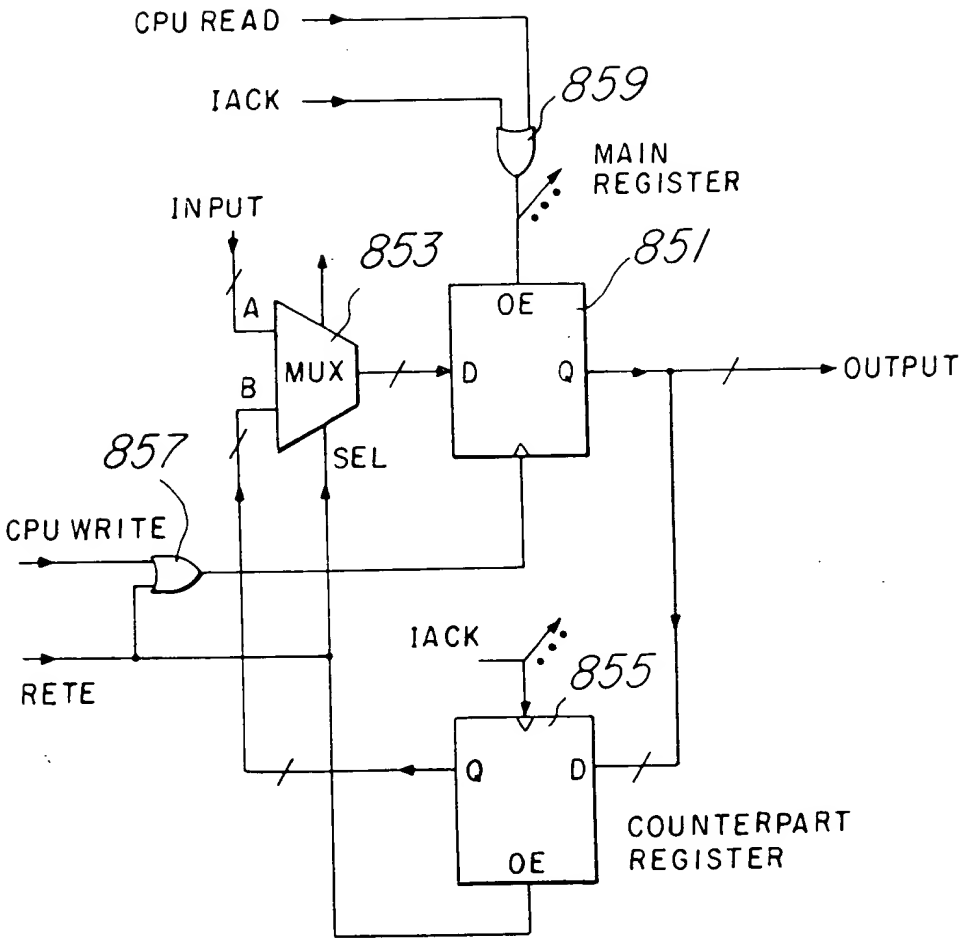

Fig. 22

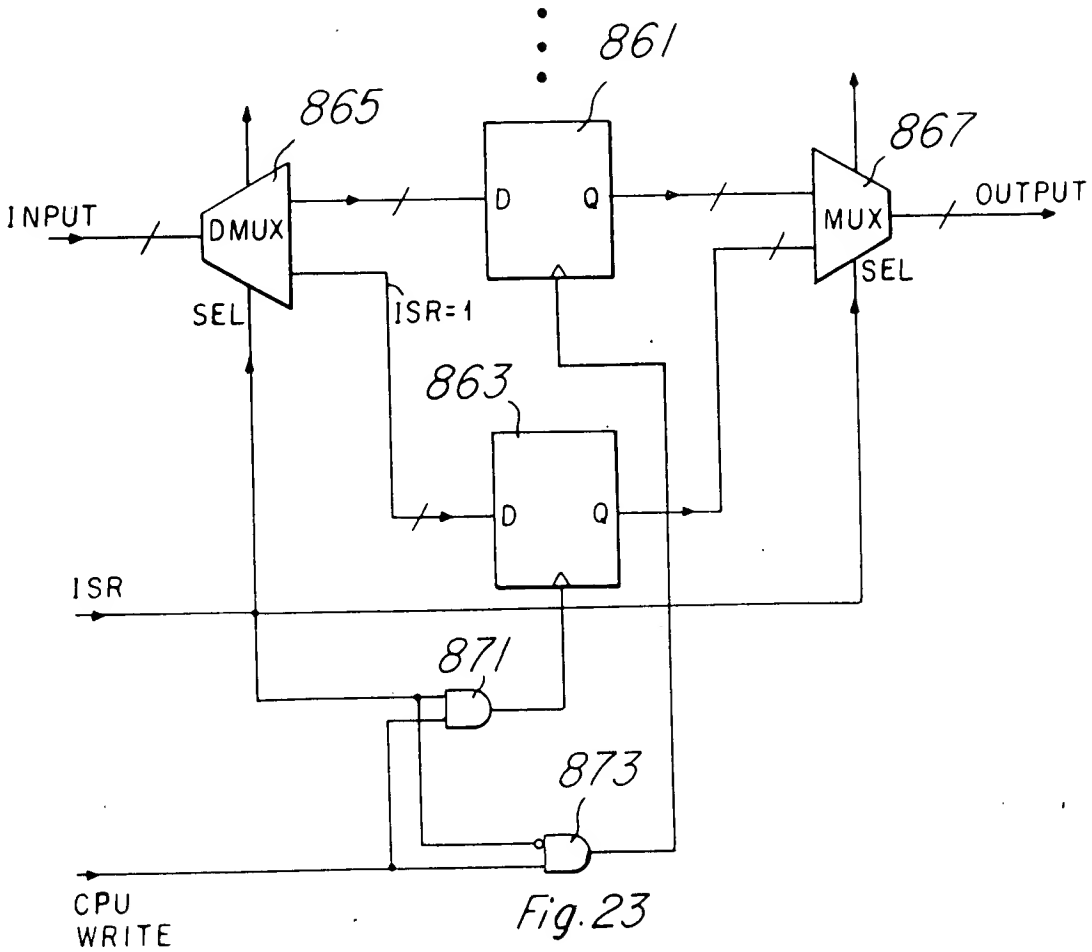
861
865
867
INPUT
DMUX
D
Q
MUX
OUTPUT
SEL
ISR=1
SEL
863
D
Q
ISR
871
873
CPU
WRITE

Fig. 23

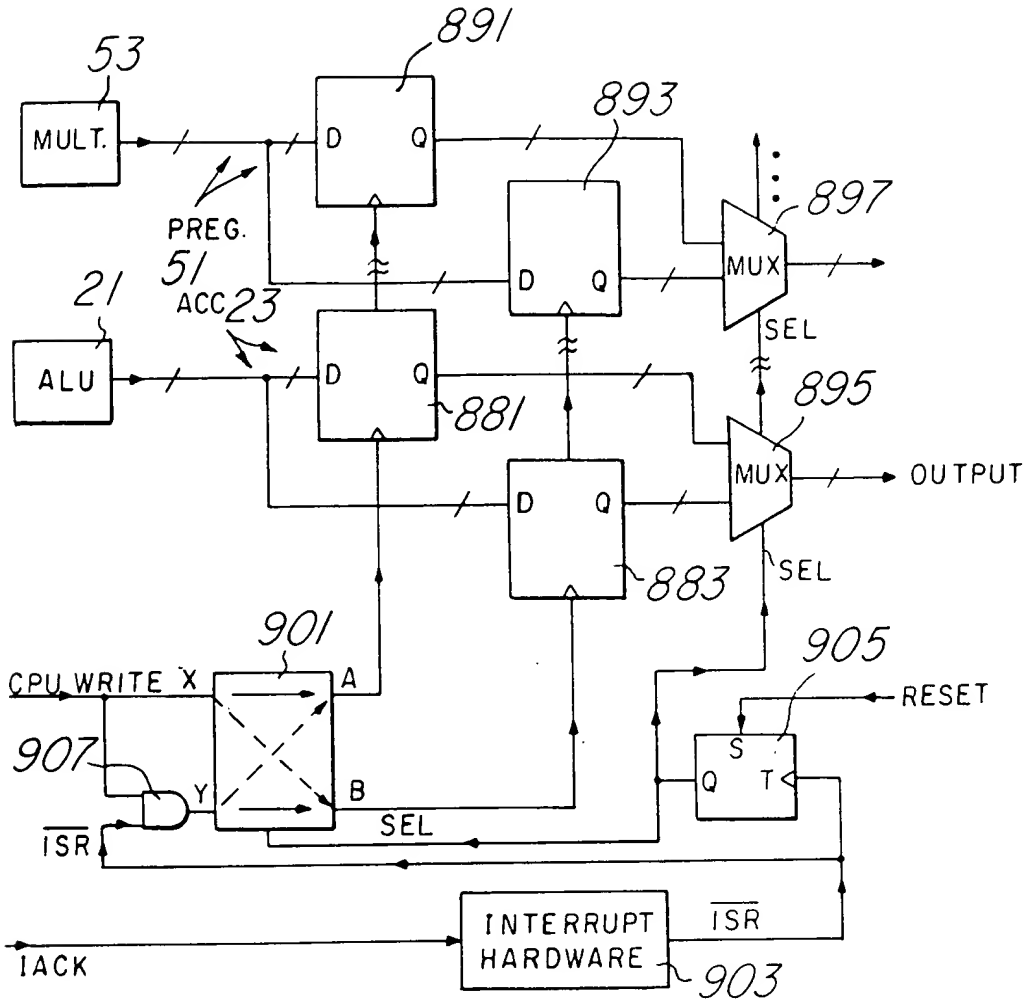
53
MULT.
891
D
Q
893
PREG.
51
ACC
23
897
MUX
SEL
21
ALU
881
895
MUX
OUTPUT
883
SEL
901
905
CPU WRITE X
A
RESET
907
S
Q
T
Y
B
SEL
ISR
INTERRUPT HARDWARE
ISR
IACK
903

Fig. 24

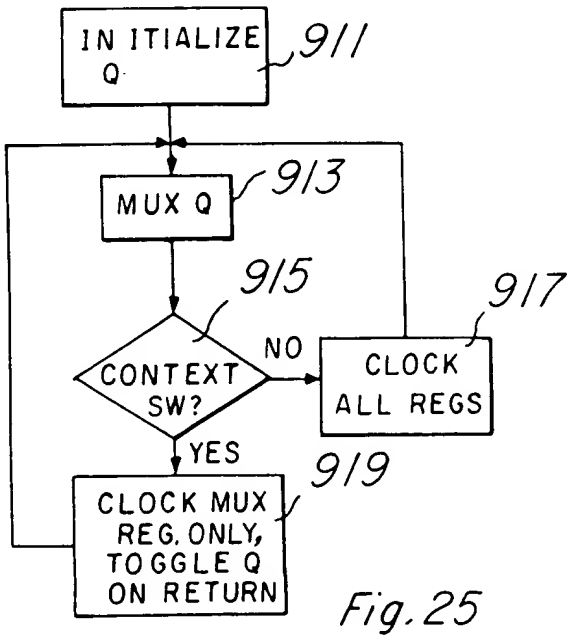
IN ITIALIZE Q
911
MUX Q
913
915
917
CONTEXT SW?
NO
CLOCK ALL REGS
YES
919
CLOCK MUX REG. ONLY, TOGGLE Q ON RETURN

Fig. 25

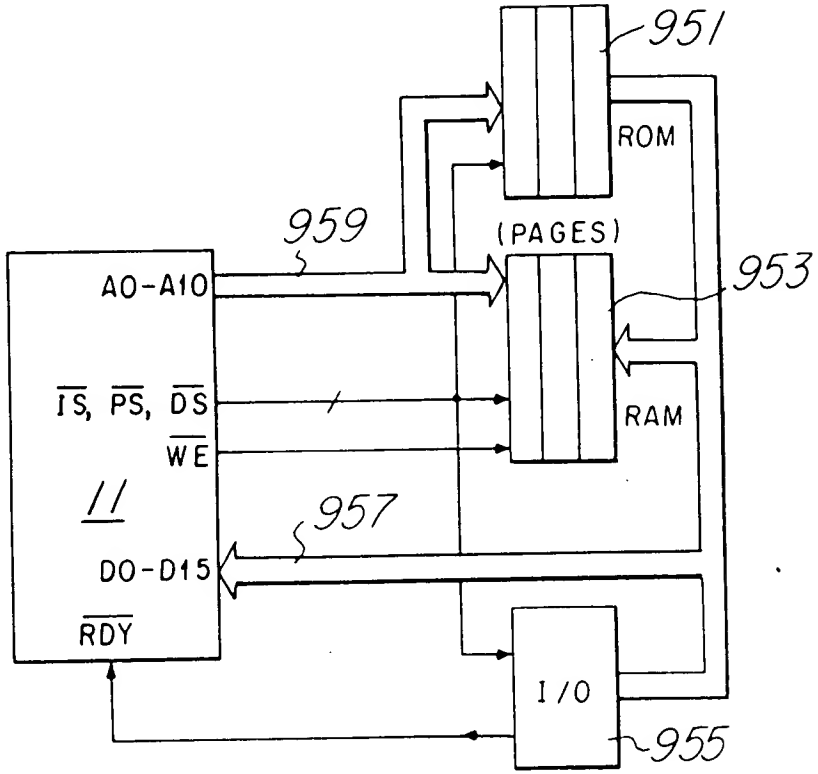

Fig. 26

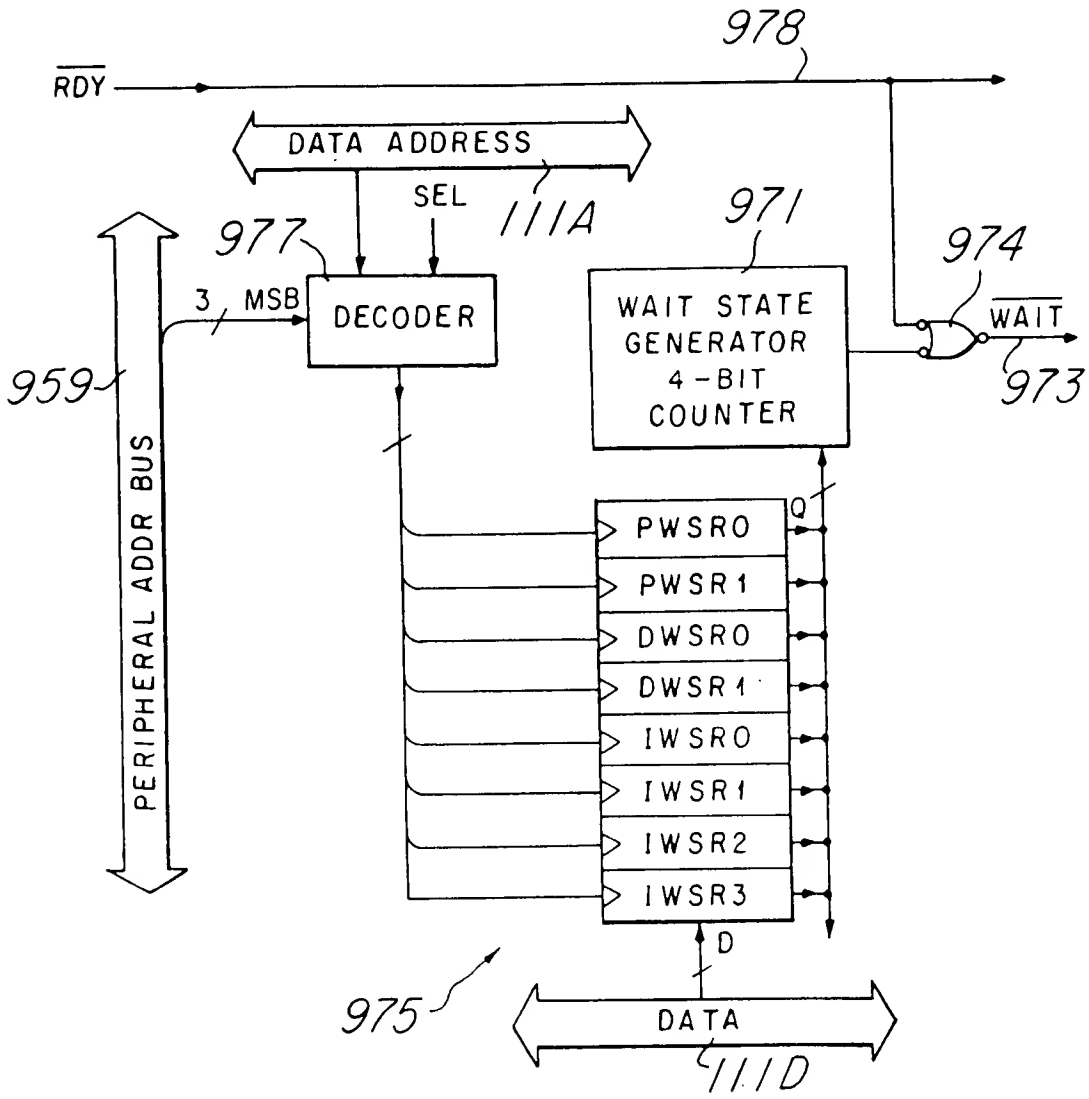
978
RDY
DATA ADDRESS
SEL
111A
971
977
974
3 MSB
DECODER
WAIT STATE GENERATOR 4-BIT COUNTER
WAIT
959
973
PERIPHERAL ADDR BUS
Q
PWSR0
PWSR1
DWSR0
DWSR1
IWSR0
IWSR1
IWSR2
IWSR3
D
975
DATA
111D

Fig. 27

0054400

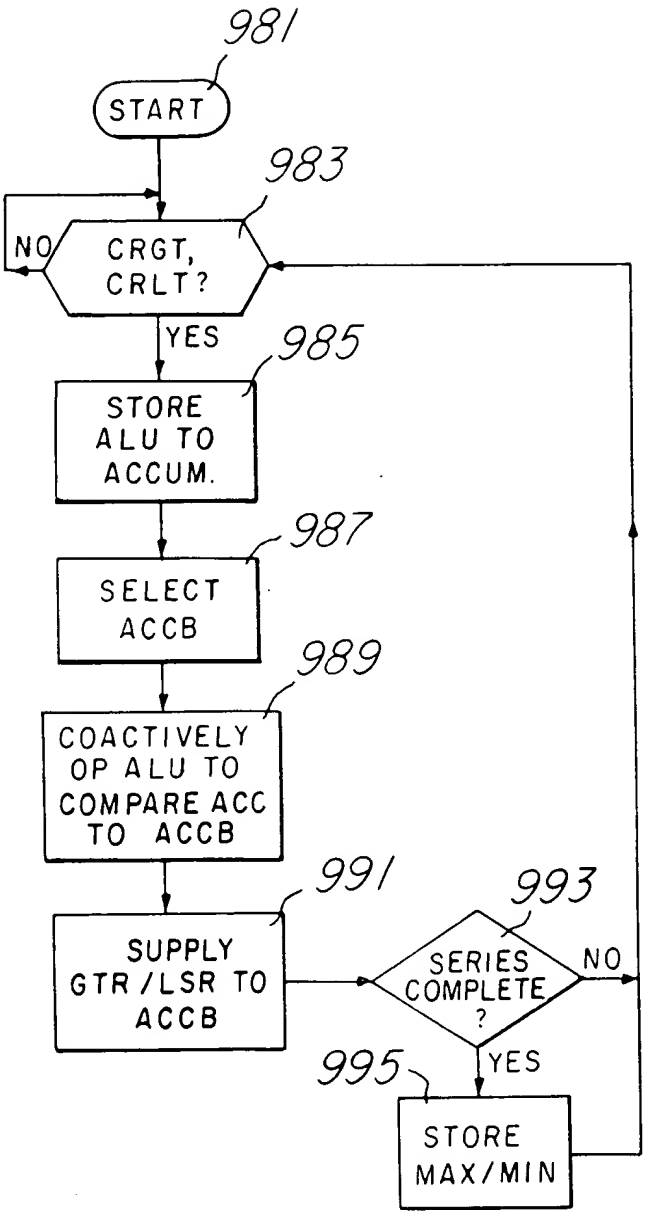

Fig. 28

00h160" 8229960

PIPELINE

INSTRUCTIONS	CYCLE 1	2	3	4	5	6	7
1	FETCH	DECODE	READ	EXECUTE			
2		FETCH	DECODE	READ	EXECUTE		
3			FETCH	DECODE	READ	EXECUTE	
4				FETCH	DECODE	READ	EXECUTE
5					FETCH	DECODE	READ

Fig. 29

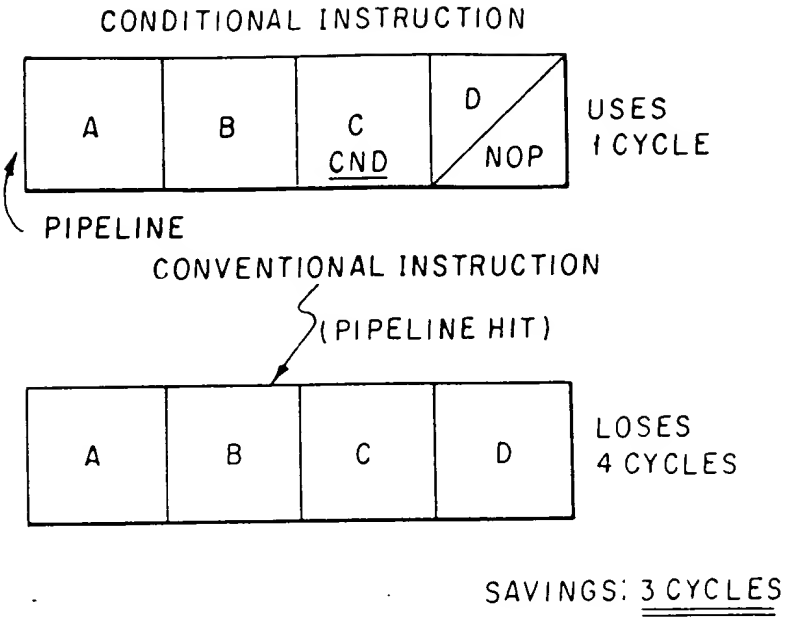
CONDITIONAL INSTRUCTION
A
B
C
CND
D
NOP
USES
1 CYCLE
PIPELINE
CONVENTIONAL INSTRUCTION
(PIPELINE HIT)
A
B
C
D
LOSES
4 CYCLES
SAVINGS: 3 CYCLES

Fig. 30

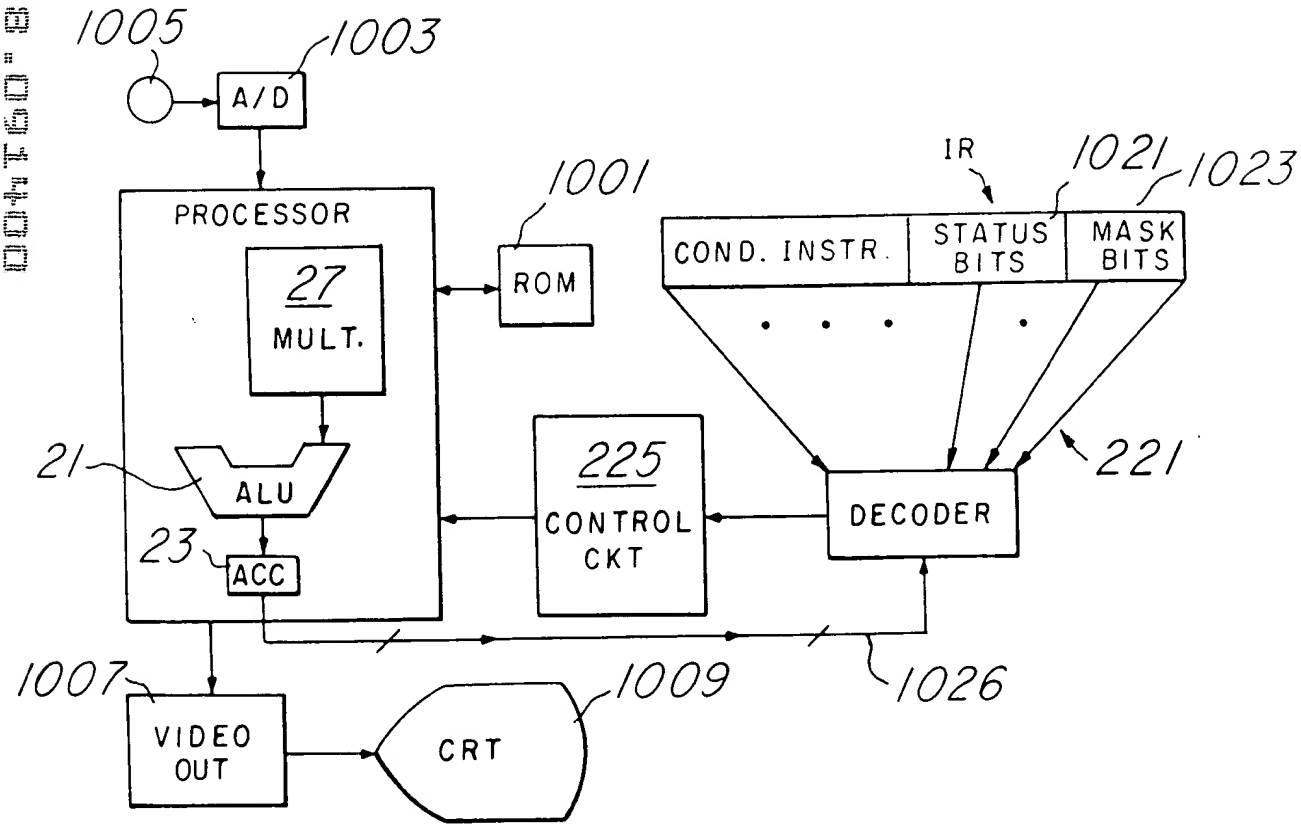
1005
1003
A/D
PROCESSOR
27
MULT.
1001
ROM
IR
1021
1023
COND. INSTR.
STATUS BITS
MASK BITS
21
ALU
23
ACC
225
CONTROL CKT
DECODER
221
1007
VIDEO OUT
CRT
1009
1026

Fig. 31

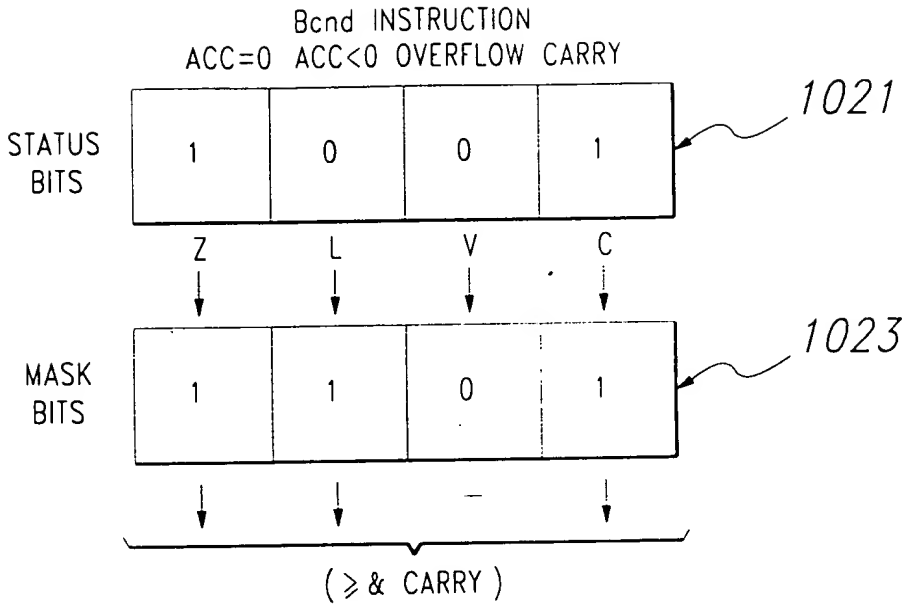
Bcnd INSTRUCTION
ACC=0 ACC<0 OVERFLOW CARRY
STATUS BITS
1
0
0
1
1021
Z
L
V
C
MASK BITS
1
1
0
1
1023
(≥ & CARRY)

Fig. 32

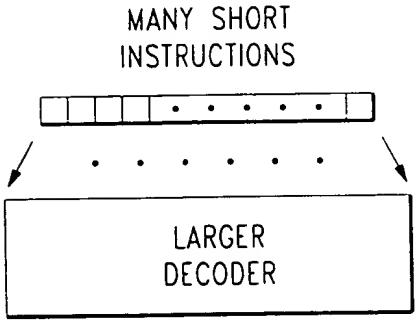
MANY SHORT INSTRUCTIONS
LARGER DECODER

Fig. 33

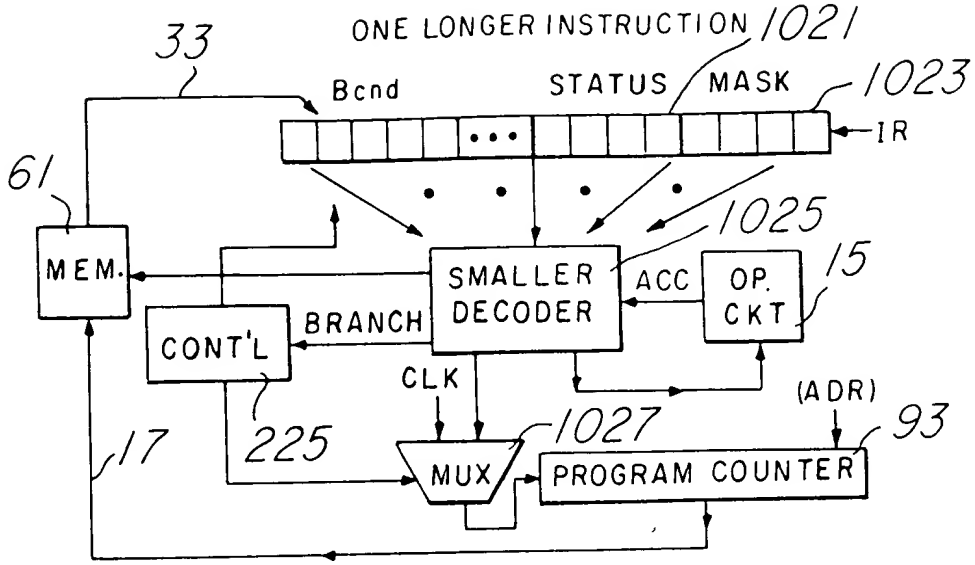
33
ONE LONGER INSTRUCTION
1021
Bcnd
STATUS
MASK
1023
IR
61
1025
MEM.
SMALLER DECODER
ACC
OP. CKT
15
CONT'L
BRANCH
CLK
(ADR)
93
17
225
1027
MUX
PROGRAM COUNTER

Fig. 34

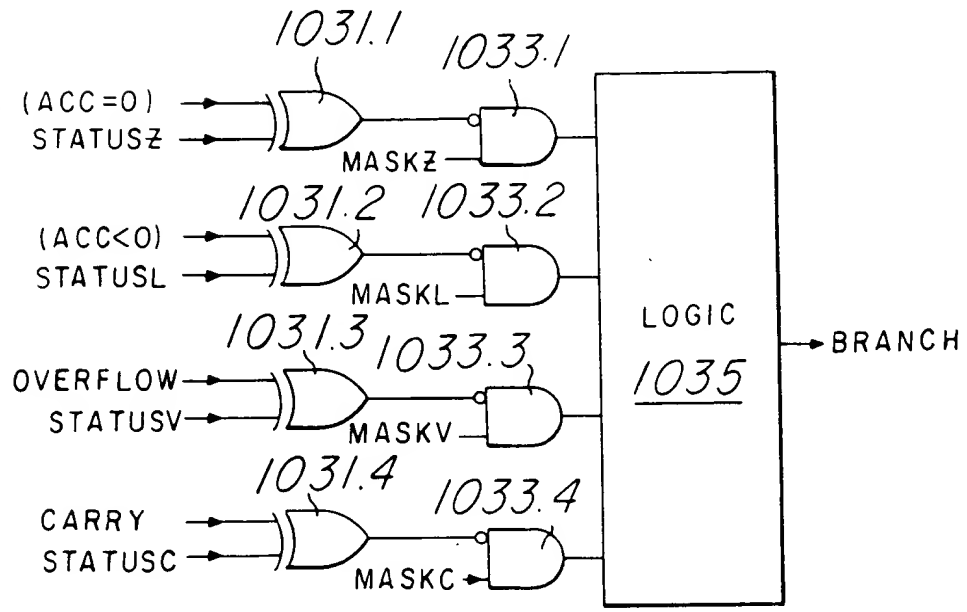
1031.1
1033.1
(ACC=0)
STATUSZ
MASKZ
1031.2
1033.2
(ACC<0)
STATUSL
MASKL
LOGIC
1035
BRANCH
1031.3
1033.3
OVERFLOW
STATUSV
MASKV
1031.4
1033.4
CARRY
STATUSC
MASKC

Fig. 35

0062328 - 062400

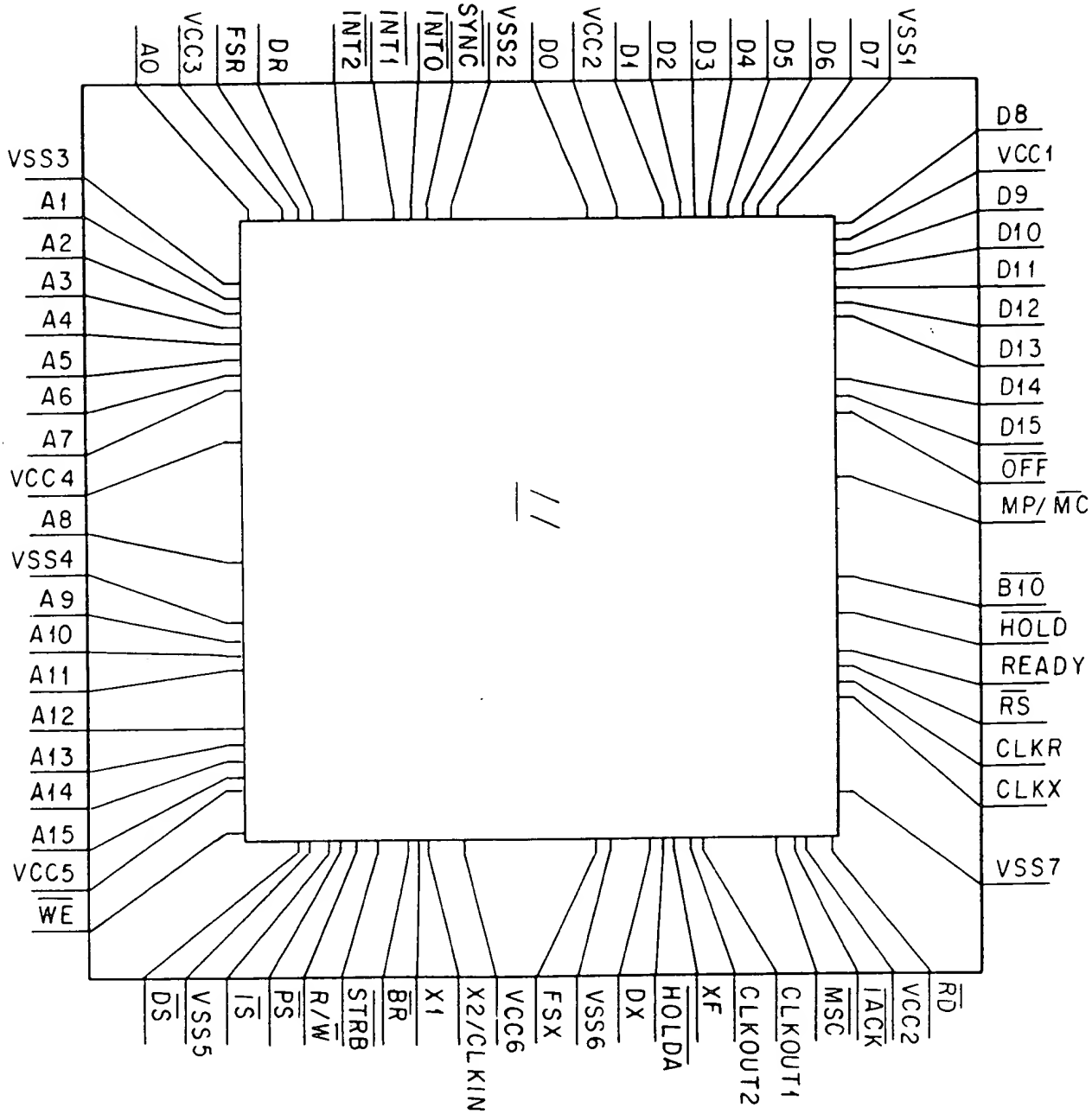

Fig. 36

00460 8222960

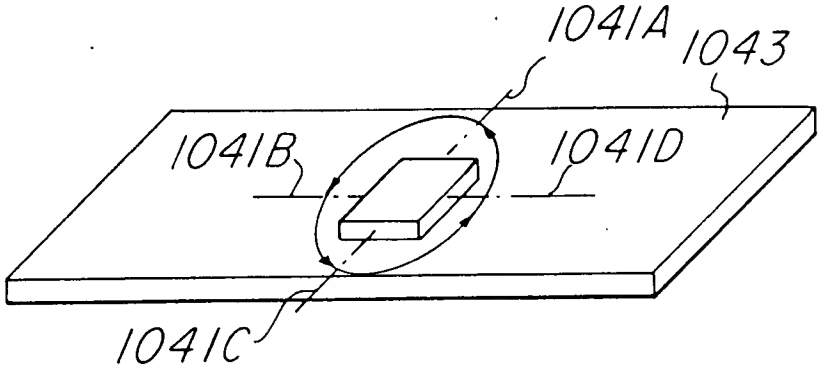

Fig.37

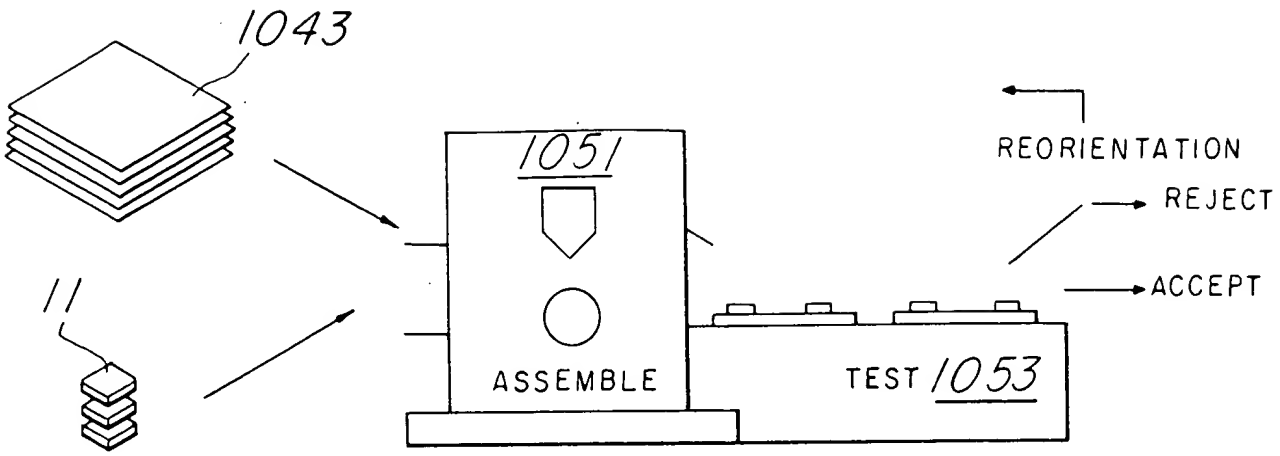
1043
1051
REORIENTATION
REJECT
ACCEPT
11
ASSEMBLE
TEST 1053

Fig. 38

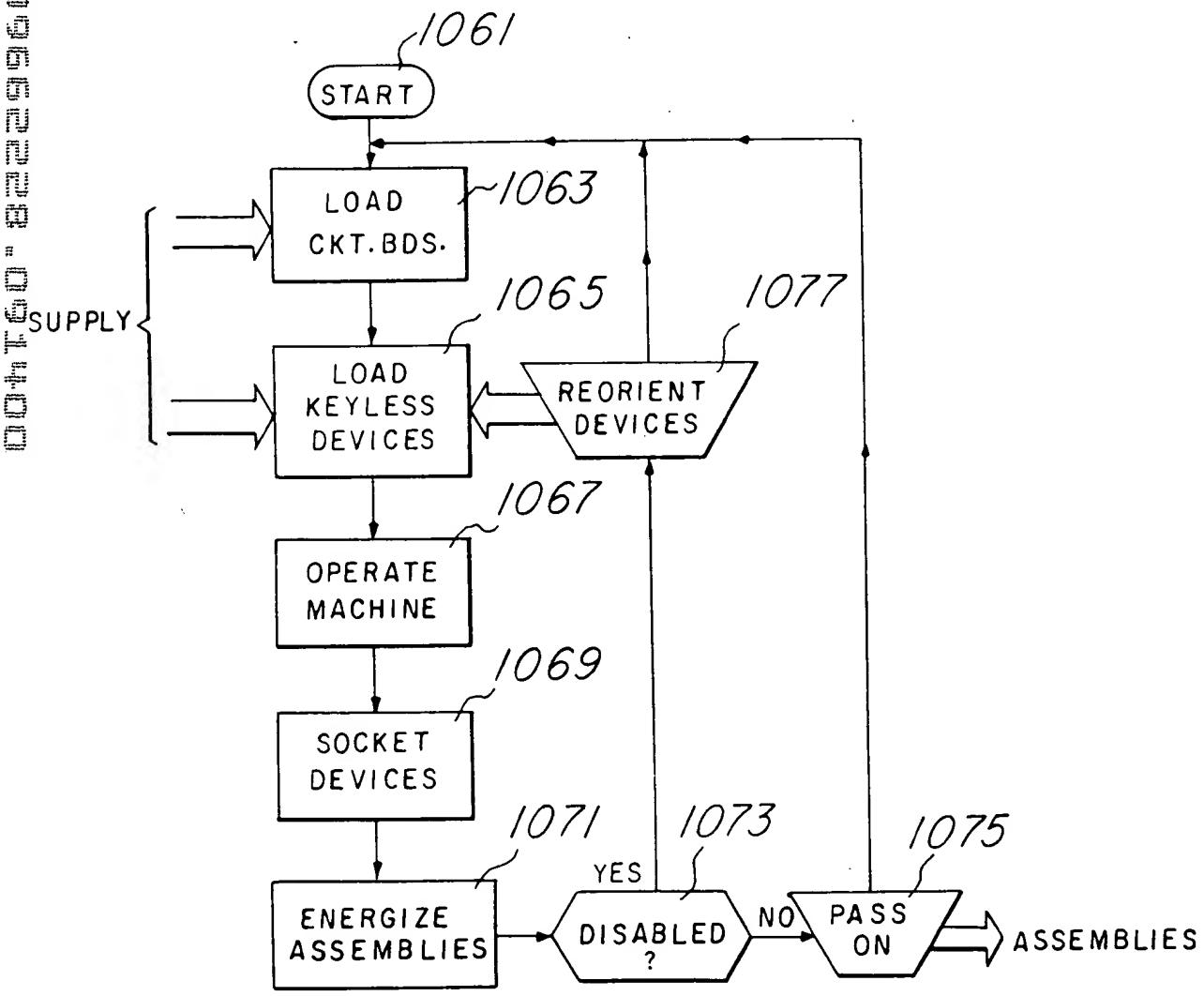
1061
START
LOAD CKT. BDS.
1063
SUPPLY
1065
LOAD KEYLESS DEVICES
1077
REORIENT DEVICES
1067
OPERATE MACHINE
1069
SOCKET DEVICES
1071
ENERGIZE ASSEMBLIES
1073
YES
DISABLED ?
NO
1075
PASS ON
ASSEMBLIES

Fig. 39

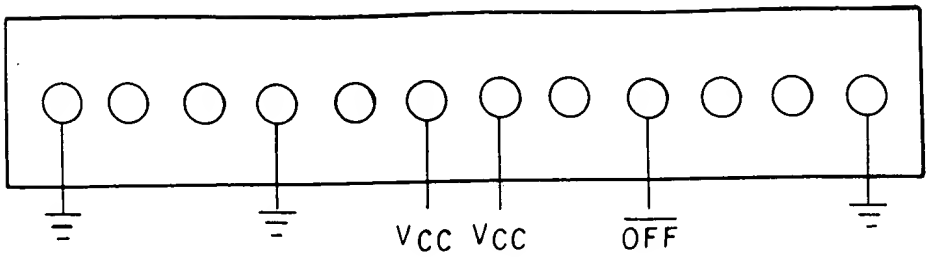

Fig. 40

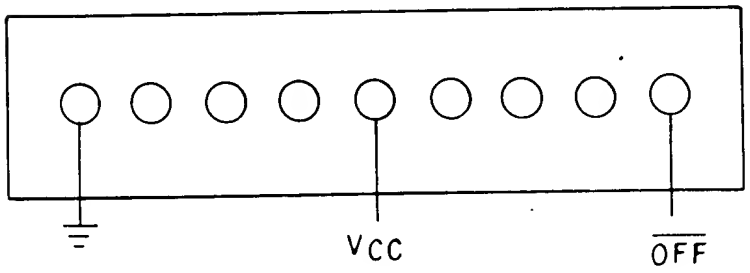

Fig. 41

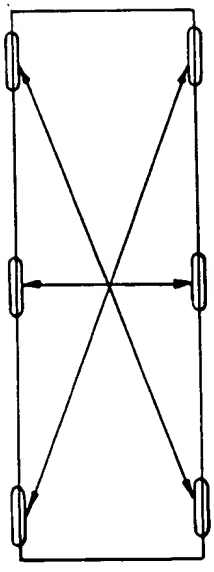

Fig. 42

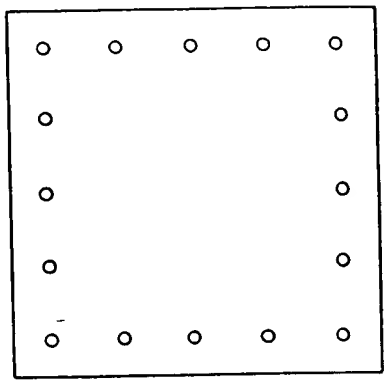

Fig. 43

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